LINEAR WAVESHAPING

Introduction:

If a circuit is designed with components like R ,L and C then it is called linear circuit. When sinusoidal signal is applied ,the shape of the signal is preserved at the output with or without change in the amplitude and shape. But a non-sinusoidal signal alters the output when it is transmitted through a linear circuit.

The process whereby the form of non-sinusoidal signals such as step, pulse, square wave, ramp and exponential is altered by transmission through a linear network is called linear wave shaping.

HIGHPASS RC CIRCUIT

Consider high pass RC circuit as shown in fig.1 below.

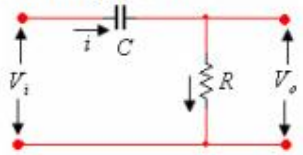


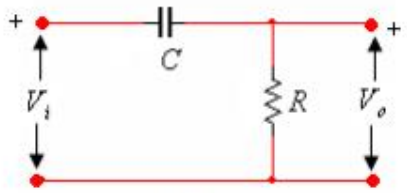
Fig.1 Highpass RC circuit

The capacitor offers high reactance at low frequency and low reactance at high frequency. Hence low frequency components are not transmitted ,but high frequencies are with less attenuation. Therefore the output is large and the circuit is called a high pass circuit.

Let us see now is, what will be the response if different types of inputs, such as, sinusoidal ,step, pulse, square wave, exponential and ramp are applied to a highpass circuit., like?

(i) Sinusoidal input

First consider the response of a highpass RC circuit.



$$V_o = V_i \frac{R}{R + 1/j\omega C}$$

$$\left|\frac{V_o}{V_i}\right| = \frac{R}{\sqrt{R^2 + \left(\frac{1}{\omega C}\right)^2}} = \frac{R}{R\sqrt{1 + \left(\frac{1}{\omega CR}\right)^2}} = \frac{1}{\sqrt{1 + \left(\frac{1}{\omega CR}\right)^2}}$$

Let $\omega_1 = \frac{1}{CR}$

$$\left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{1 + \left(\frac{\omega_1}{\omega}\right)^2}}$$

At $\omega = \omega_1$

$$\left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{2}} = 0.707$$

Hence, f_1 is the lower cut -off frequency of the highpass circuit.

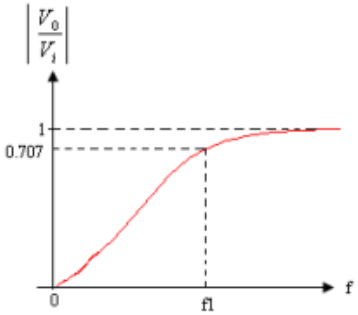


fig.2 frequency response curve for sinusoidal input.

(ii) Step input

A Step voltage is defined as,

$V_i = 0$ for $t < 0$

and $V_i = V$ for $t \geq 0$

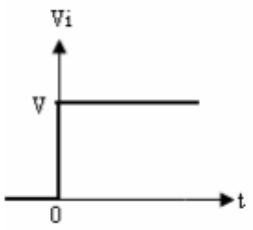


fig.3 Step Voltage

The output voltage is of the form

$V_o = B_1 + B_2 e^{-t/\tau}$

where $\tau = RC$, the time constant of the circuit.

B_1 is the steady state value as $t \to \infty$, and hence $V_o \to B_1$

Let the final value be which we denote as V_f.

Then $V_f = B_1$

B_2 is determined by the initial output voltage.

At $t = 0$, $V_i = V_o = B_1 + B_2$

Therefore, $B_2 = V_i - B_1$

$= V_i - V_f$

Hence the general solution is

$$V_o = V_f + (V_i - V_f) e^{-t/\tau}$$

Fall time t_f: When a step is applied, the time taken for the output voltage to fall from 90%of its initial value to 10% of its initial value is the fall time. It indicates how fast the output reaches its steady state value.

The output voltage at any instant of time, in highpass circuit, is given by

$V_o(t) = Ve^{-t/\tau}$, At $t = t_1$, $V_o(t_1) = 90\%$ of $V = 0.9V$

$0.9 = e^{-t_1/\tau}$

$e^{t_1/\tau} = 1/0.9 = 1.11$

$t_1 / \tau = \ln(1.11)$

$t_1 = \tau \ln(1.11) = 0.1\,\tau$

At $t = t_2$, $V_o(t) = 10\%$ of $V = 0.1V$

$0.1 = e^{-t_2/\tau}$

$e^{t_2/\tau} = 1/0.1 = 10$

$t_2 = \tau \ln(10) = 2.3\,\tau$

$\therefore$ fall time, $t_f = t_2 - t_1 = 2.3\tau - 0.1\tau = 2.2\,\tau$

The lower half power frequency of the highpass circuit is

$$f_1 = \frac{1}{2\pi RC}$$

$$\tau = RC = \frac{1}{2\pi f_1}$$

$$\text{Fall time} = t_f = 2.2\,\tau = \frac{2.2}{2\pi f_1} = \frac{0.35}{f_1}$$

Hence, the fall time is inversely proportional to f_1, the lower cut-off frequency.

(iii) Pulse input: A pulse can be expressed as combination of a positive(negative) step followed by negative(positive) step w.r.t. times i.e.

$V_i = V_u(t) - V_u(t - t_p)$ where t_p is the duration of the pulse as shown below in fig.5

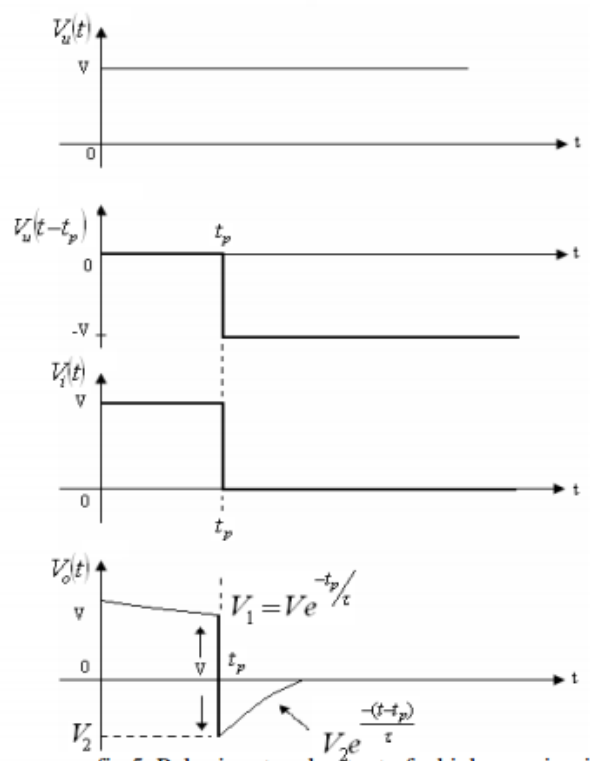


fig.5 Pulse input and output of a highpass circuit

Consider a pulse signal is applied to the input of a high pass circuit.

At t=0, V_i abruptly rises to V . As the capacitor is connected between the input and output, the output also changes by the same amount. As the input remains constant, the output decays exponentially to V_1 at $t = t_p$.

Therefore, $V_1 = Ve^{-t_p/\tau}$

At $t = t_p$, the input abruptly falls by V. V_o also falls by the same amount.

At $t = t_p$, $V_o = V_1 - V$

Since V_1 is less than V , V_o is negative and its value is V_2 and this decays to zero exponentially.

For $t > t_p$, $V_o = (V_1 - V)e^{-(t-t_p)/\tau}$

But $V_1 = Ve^{-t_p/\tau}$

$$\therefore V_o = V(e^{-t_p/\tau} - 1)\, e^{-(t-t_p)/\tau}$$

The response of a highpass circuit with pulse input for different values of τ is plotted in fig.1.6.

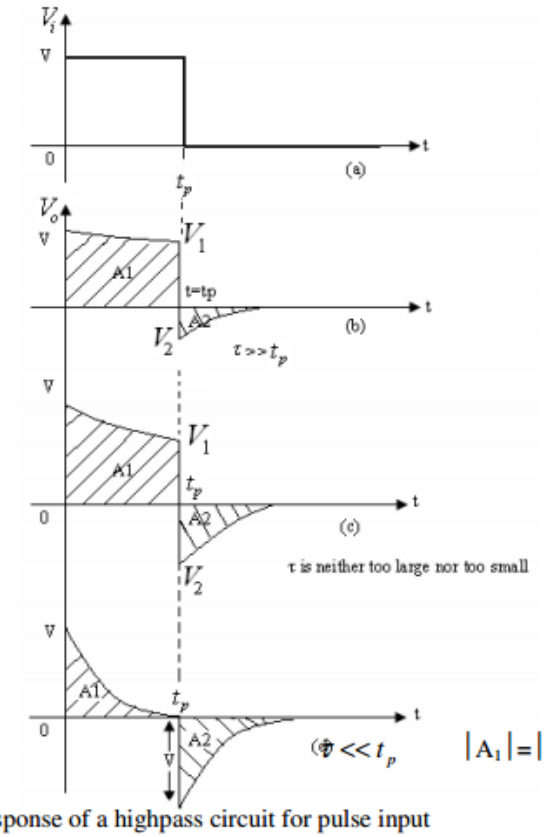


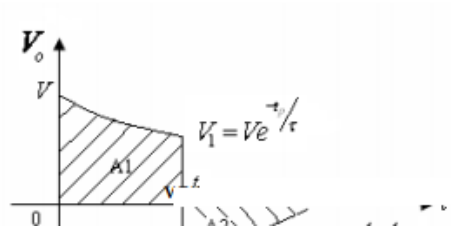
Fig.6 Response of a highpass circuit for pulse input

It is very clear that output has distortion when a pulse is passing through a high pass RC circuit. The shape of the pulse at the output is almost preserved when the time constant τ is very large (fig.6b) whereas in fig.6c there is a tilt at the top of the pulse and an undershoot at the end of the pulse.

If $\tau << t_p$ (fig.1.6d), the output consists of a positive spike at the beginning of the pulse and a negative spike at the end of the pulse, that means a highpass circuit converts a pulse into spikes called 'peaking'. To have a less distortion,τ must be very much larger than the time period of the input pulse. In general, there is an undershoot at the end of the pulse. The area above the axis(A_1) is always equal to the area below (A_2).

Area A_1: $0 < t < t_p$

$$V_o = Ve^{-t/\tau}$$



$$A_1 = \int_0^{t_p} V e^{-t/\tau} dt = \left[-V\tau e^{-t/\tau} \right]_0^{t_p}$$

Fig.7 Calculation of A_1 and A_2

$$A_1 = \left[-V\tau e^{-t_p/\tau} + V\tau \right] = V\tau(1 - e^{-t_p/\tau})$$

Similarly

$$A_2 = \int_{t_p}^{\infty} V(e^{-t_p/\tau} - 1) e^{-(t-t_p)/\tau} dt$$

$$= \int_{t_p}^{\infty} \left[V e^{-t/\tau} - V e^{-(t-t_p)/\tau} \right] dt$$

$$= \left[\frac{V e^{-t/\tau}}{-1/\tau} \right]_{t_p}^{\infty} - \left[V \frac{1}{-1/\tau} e^{-(t-t_p)/\tau} \right]_{t_p}^{\infty}$$

$$A_2 = \left[V\tau e^{-t_p/\tau} - V\tau \right] = -V\tau(1 - e^{-t_p/\tau})$$

$|A_1| = |A_2|$

(iv) Squarewave-Average level

A waveform that has a constant amplitude $V^{'}$ for a time T_1 and has another constant amplitude $V^{'}$ for a time T_2 and which is repetitive with a time T= (T_1+ T_2) is called a square wave. If T_1= T_2 = $\frac{T}{2}$, then it is called a symmetric squarewave and the typical input-output waveforms of the highpass circuit are shown in fig.8.

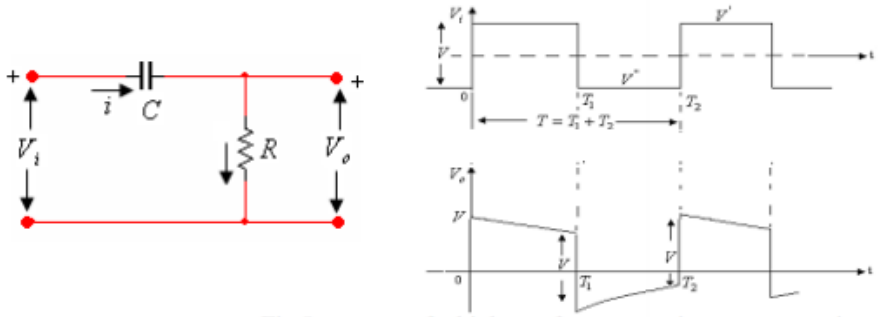


Fig.8 output of a highpass for symmetric square wave input

Whatever is the dc component associated with the periodic input, waveform the dc level of the steady state output signal for the highpass circuit is always zero.
This can be verified by using KVL equation

$V_i = \frac{q}{C} + V_o$ where q is the capacitor charge

Differentiating with respect to t

$$\frac{dV_i}{dt} = \frac{1}{C}\frac{dq}{dt} + \frac{dV_o}{dt}$$

But i = $\frac{dq}{dt}$

Substituting above condition

$$\frac{dVi}{dt} = \frac{i}{C} + \frac{dV_o}{dt}$$

Since $V_o = iR, \quad i = \frac{V_o}{R} \quad and \quad RC = \tau$

$$\therefore \frac{dV_i}{dt} = \frac{V_o}{\tau} + \frac{dV_o}{dt}$$

Multiplying by dt and integrating over the time period T we get

$$\int_0^T dV_i = \left[V_i\right]_0^T = V_i(T) - V_i(0)$$

$$\int_0^T \frac{V_o}{\tau} dt = \frac{1}{\tau}\int_0^T V_o dt$$

$$\int_0^T dV_o = \left[V_o\right]_0^T = V_o(T) - V_o(0)$$

From above eqns

$$V_i(T) - V_i(0) = \frac{1}{\tau}\int_0^T V_o dt + \left[V_o(T) - V_o(0)\right]$$

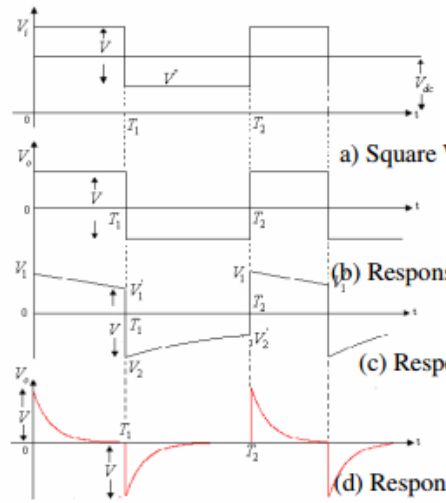
Under steady-state conditions, the output and the input waveform are repetitive with a time period T. Therefore, $V_i(T) = V_o(T)$ and $V_i(0) = V_o(0)$

$$\int_0^T V_o dt = 0$$

Since this integral represents the area under the output waveform over one cycle,it is evident that the dc in the steady state is always zero.

Square wave Response

Now consider the response of the highpass RC circuit for a square wave input for different values of the time constant, τ , fig.9.



a) Square Wave input

(b) Response $\tau >> T_1$ and $\tau >> T_2$

(c) Response When τ is neither too large nor too small

(d) Response when τ is very small

Fig.9 Response of a highpass circuit for square input

Consider the typical response of the highpass circuit for square wave input, fig.10

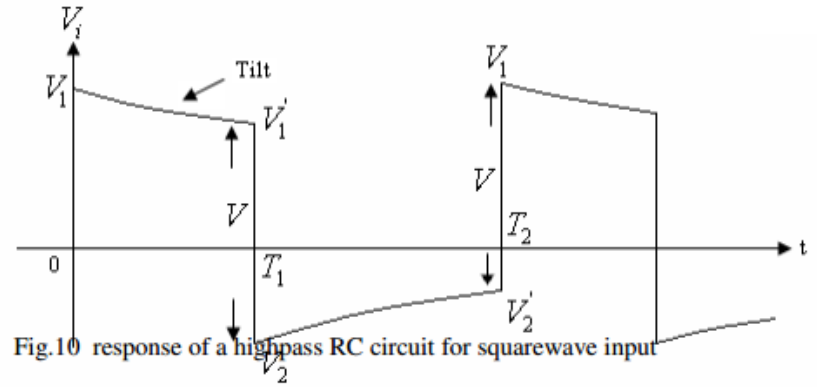


Fig.10 response of a highpass RC circuit for squarewave input

We know that $V_1' = V_1 e^{-T_1/\tau}$ and $V_1' - V_2 = V$

And $V_2' = V_2 e^{-T_2/\tau}$ and $V_1 - V_2' = V$

For a symmetric squarewave $T_1 = T_2 = \frac{T}{2}$

And because of symmetry $V_1 = -V_2$ *and* $V_1' = -V_2'$

From equation $V_1' - V_2 = V$

But $V_1' = V_1 e^{-T_1/\tau}$

Therefore $V_1 e^{-T_1/\tau} - V_2 = V$

From $V_1 = -V_2$

Substituting ,we have

$$V_1 e^{-T_1/\tau} + V_1 = V$$

$$V_1(1+e^{-T_1/\tau}) = V$$

Thus, $$V_1 = \frac{V}{1+e^{-T_1/\tau}}$$

For a symmetric squarewave as $T_1 = T_2 = \frac{T}{2}$,

therefore $$V_1 = \frac{V}{1+e^{-T/2\tau}}$$

But $V_1^{'}$ = $V_1 e^{-T/2\tau}$

$$V_1^{'} = V\frac{e^{-T/2\tau}}{(1+e^{-T/2\tau})}$$

There is a tilt in the output waveform. The percentage tilt is defined as

$$\% \text{ Tilt} = P = \frac{V_1 - V_1^{'}}{V/2} \times 100\,\%$$

$$P = \frac{\frac{V}{1+e^{-T/2\tau}} - \frac{Ve^{-T/2\tau}}{1+e^{-T/2\tau}}}{V/2} \times 100\%$$

If $\frac{T}{2\tau} << 1$

$P \cong \frac{T}{2\tau} \times 100\%$ since $\frac{T}{2t} << 1$

$P = \frac{T}{2\tau} \times 100\,\%$, for a symmetrical squarewave

The lower cut-off frequency, $f_1 = \frac{1}{2\pi\tau}$

Therefore $\frac{1}{2\tau} = \pi f_1$

$P = \pi f_1 T \times 100\%$

Therefore, $P = \frac{\pi f_1}{f} \times 100\%$, since $T = \frac{1}{f}$

(vi) Ramp input: Ramp waveform is one which increases linearly with time for t> 0 and is zero for t<0.

Let the input to the highpass circuit be $V_i = \alpha t$ where α is the slope fig.13

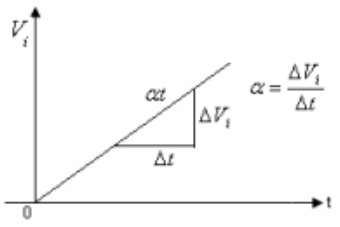


fig.13 ramp input

For the highpass circuit, we have

$$V_i = \frac{1}{\tau}\int V_o dt + V_o$$

$$\alpha t = \frac{1}{\tau}\int V_o dt + V_o$$

solving for V_o

$$V_o(t) = \alpha\tau\left[1 - e^{\frac{-t}{\tau}}\right]$$

If $\frac{t}{\tau} << 1$

$$e^{\frac{-t}{\tau}} = 1 - \frac{t}{\tau} + \frac{t^2}{2\tau^2}$$

Therefore $V_o(t) = \alpha\tau\left[1 - 1 + \frac{t}{\tau} - \frac{t^2}{2\tau^2}\right]$

$$V_o(t) = \alpha t\left[1 - \frac{t}{2\tau}\right]$$

The output falls away from the input, fig.14

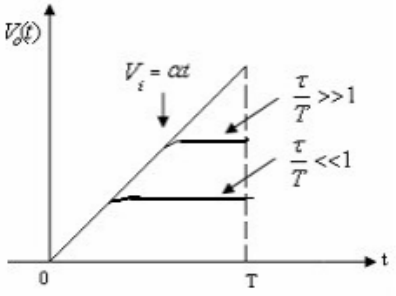


Fig. 14 Response of a highpass circuit to ramp input

Transmission error is defined as the deviation from linearity and is given by

$$e_t = \frac{V_i - V_o}{V_i}$$

$$V_i = \alpha t$$

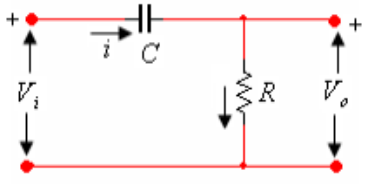
At t = T, $V_i = \alpha T$, And $V_o = \alpha T\left(1-\frac{T}{2\tau}\right)$

Therefore $e_t = \frac{\alpha T - \alpha T(1-\frac{T}{2\tau})}{\alpha T} = \frac{\frac{\alpha T^2}{2\tau}}{\alpha T} = \frac{T}{2\tau}$

Thus, $e_t = \frac{T}{2\tau} = \prod f_1 T \ as \frac{1}{2\tau} = \pi f_1$

HighPass RC Circuit as Differentiator

If the time constant of the RC highpass circuit is very much smaller than the time period of the input signal, then the circuit behaves as a differentiator. Then the voltage drop across R is very small when compared to the drop across C.



$$V_i = \frac{1}{C}\int i\,dt + iR$$

But $iR = V_o$ is small

Therefore $V_i = \frac{1}{C}\int i\,dt$

$$i = \frac{V_o}{R}$$

$$\therefore V_i = V_i = \frac{1}{\tau}\int V_o\,dt = \frac{1}{\tau}\int V_o\,dt$$

Differentiating

$$\frac{dV_i}{dt} = \frac{V_o}{\tau}$$

$$V_o = \tau\frac{dV_i}{dt}$$

$$\therefore V_o \propto \frac{dV_i}{dt}$$

The output is proportional to the differential of the input signal, fig.15

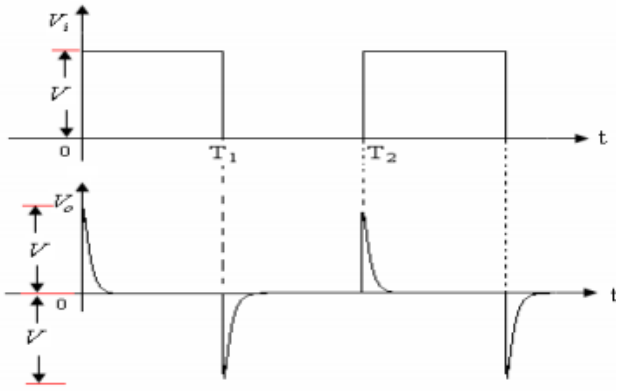


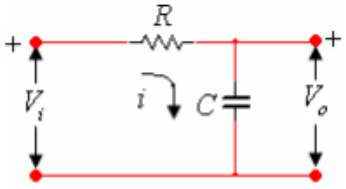
fig.15 output of a differentiator

LOWPASS CIRCUITS,

Introduction:

Low pass circuit is one which allows low frequencies with less attenuation and high frequencies with maximum attenuation. This is because capacitance offers high reactance at low frequencies and hence there is an output.

LOWPASS RC CIRCUIT: Following is the lowpass RC circuit.



(a)

Lowpass RC Circuit

At low frequencies the reactance of C is large and as frequency increases its reactance decreases. Hence the output is larger for smaller frequencies and is smaller for larger frequencies. Hence this circuit is called a lowpass circuit. Cosider the response of this circuit for different types of inputs.

i) SINUSOIDAL INPUT: For the circuit shown above, if sinusoidal signal is applied as an input, the output V_o is given by

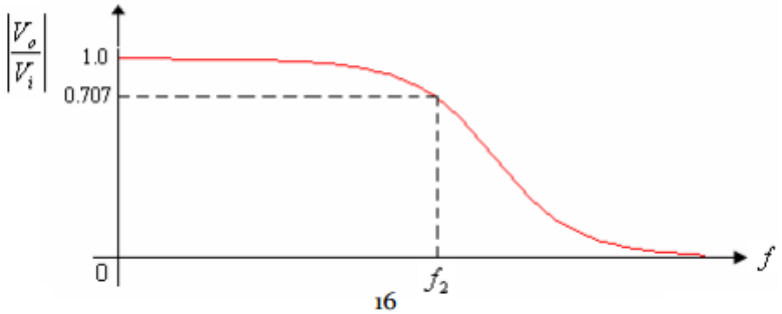
$$V_o = V_i \frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}}$$

$$\frac{V_o}{V_i} = \frac{1}{1 + j\omega CR}$$

$$\left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{1+(\omega CR)^2}} = \frac{1}{\sqrt{1+\left(\frac{\omega}{\omega_2}\right)^2}} \qquad \text{,where } \omega_2 = \frac{1}{CR}$$

At $\omega = \omega_2$, $\left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{2}} = 0.707$

Hence, f_2 is the upper cut-off frequency as shown in the response curve below.



(ii) STEP INPUT: When a step voltage is applied as input to the lowpass circuit the output will be appeared as shown in fig. Below.

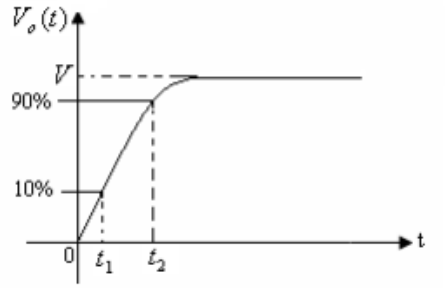
We have $RC = \tau$

$$V_o = V_f + (V_i - V_f)e^{\frac{-t}{\tau}}$$

Here, $V_f = V$ and $V_i = 0$

$$\therefore V_o(t) = V - Ve^{\frac{-t}{\tau}} = V\left(1 - e^{\frac{-t}{\tau}}\right)$$

As $t \to \infty$, $V_o(t) \to V$



Response of lowpass circuit to step input

On the otherhand, the output can be obtained by solving the differential equation.

$$V = V_i = Ri + \frac{1}{C}\int idt$$

We know that $\frac{1}{C}\int idt = V_o$

$$\frac{i}{C} = \frac{dV_o}{dt}$$

$$i = C\frac{dV_o}{dt}$$

$$V = RC\frac{dV_o}{dt} + V_o$$

$$V = \tau\frac{dV_o}{dt} + V_o$$ Solving for

$$V_o(t) = V_o = V - Ve^{\frac{-t}{\tau}} = V\left(1 - e^{\frac{-t}{\tau}}\right)$$

Rise time: The time taken for the output to reach from 10% of its final value to 90% of its final value is called rise time.

Fom equation

$$\frac{V_o}{V} = 1 - e^{\frac{-t}{\tau}}$$

From fig. at $t = t_1$, $V_o = 0.1V$

$$0.1 = 1 - e^{\frac{-t_1}{\tau}}$$

$$e^{\frac{-t_1}{\tau}} = 0.9$$

$$t_1 = 0.1\tau$$

Similarly at $t = t_2$, $V_o = 0.9V$

$$0.9 = 1 - e^{\frac{-t}{\tau}}$$

$$e^{-t_2/\tau} = 0.1$$

$$t_2 = 2.3\tau$$

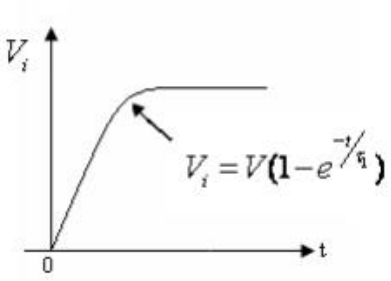
Rise time $t_r = t_2 - t_1 = 2.3\,\tau - 0.1\,\tau = 2.2\,\tau$

Also $f_2 = \dfrac{1}{2\pi RC}$

$$RC = \tau = \frac{1}{2\pi f_2}$$

$$t_r = 2.2\,\tau = \frac{2.2}{2\pi f_2} = \frac{0.35}{f_2}$$

(vi) Ramp Input:



The input is a ramp
i.e. $V_i = \alpha t$

We have $V_i = \tau \frac{dV_0}{dt} + V_0$

$\therefore \alpha t = \tau \frac{dV_0}{dt} + V_0$

solving for output, we have

$V_o(t) = -\alpha\tau + \alpha t + \alpha\tau e^{-t/\tau}$

$V_o(t) = \alpha\left[t - \tau\left(1 - e^{-t/\tau}\right)\right]$

At t = T

$V_o(T) = \alpha\left[T - \tau\left(1 - e^{-T/\tau}\right)\right]$

Case 1 : If $\tau << T$, then the deviation of the output from the input is very small since

$e^{-T/\tau} \approx 0$

$V_o(t) = \alpha(T - \tau)$

Case 2: If $\tau >> T$, then $e^{-T/\tau}$ can be expanded as series

$$V_o(t) = \alpha\left[T - \tau\left(\frac{T}{\tau} - \frac{T^2}{2\tau^2}\right)\right]$$

$$= \alpha\left[T - T + \frac{T^2}{2\tau}\right] = \frac{\alpha T^2}{2\tau} \quad \text{------} \qquad 2.36$$

The response is plotted in fig. below

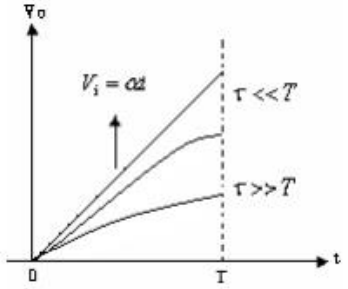


Fig. Response of lowpass circuit for ramp input

When a ramp is applied as input to a lowpass circuit, the output deviates from the input which is defined as transmission error e_t. Mathematically it can be written as

$$e_t = \frac{V_i - V_0}{V_i}$$

$$= \frac{\alpha T - \alpha(T - \tau)}{\alpha T}$$

$$e_t = \frac{\tau}{T}$$

$$f_2 = \frac{1}{2\pi\tau}$$

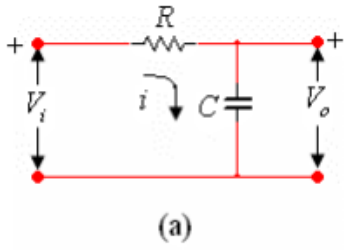
$$\tau = \frac{1}{2\pi f_2}$$

Therefore $e_t = \frac{1}{2\pi f_2} \cdot \frac{1}{T}$

Lowpass circuit as an integrator

For the lowpass circuit to behave as an integrator $\tau >> T$, then the voltage variation in C is very small

$$V_i = iR + \frac{1}{C}\int idt$$



(a)

$$V_i \cong iR$$

Since, $\frac{1}{C}\int idt << iR$

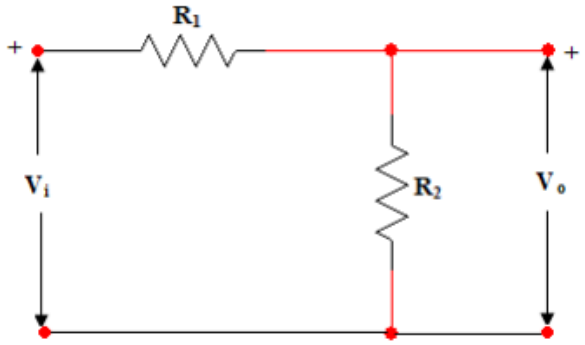
$$i = \frac{V_i}{R}$$

Therefore $V_o = \frac{1}{C}\int idt = \frac{1}{RC}\int V_i dt = \frac{1}{\tau}\int V_i dt$

The output is proportional to the integral of the input signal
Hence a lowpass circuit with large time constant produces an output that is proportional to the integral of the input.

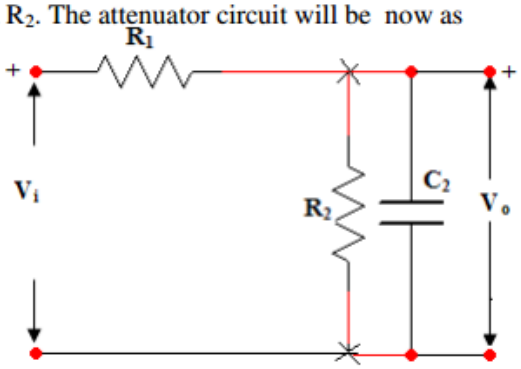
Attenuators:

An attenuator is a circuit that reduces the amplitude of the signal by a finite amount.
A simple resistance attenuator is as shown below.



Resistive Attenuator

The output is reduced depending on the choice of R_1 and R_2. The output of this attenuator can be connected as input to an amplifier having a stray capacitance C_2 and input resistance R_i.If $R_i >> R_2$, then the effective value of resistance will be smaller than R_2. The attenuator circuit will be now as



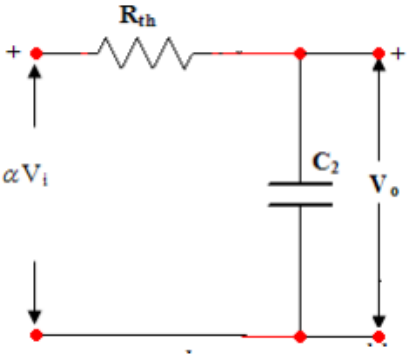
Reducing the two loop network into a single loop network by Thevenizing

$$V_{Th} = V_i \times \frac{R_2}{R_1 + R_2} = \alpha V_i \quad where\ \alpha = \frac{R_2}{R_1 + R_2}$$

and

$$R_{th} = R_1 // R_2$$

Hence the above circuit reduces to



When the input αV_i is applied to this lowpass RC circuit, the output will not reach the steady-state value instantaneously. For e.g. in the above circuit, $R_1=R_2=1M$ and $C_2 = 20nF$.Then the rise time $t_r = 2.2R_{th}C_2=2.2 \times 0.5 \times 10^6 \times 20 \times 10^{-9}$, $t_r = 22msec$. which says that approximately after a time interval of 22 msec after the application of the input αV_i to the circuit, the output reaches the steady-state value. Obviously this is an abnormally long time delay. An attenuator of this type is called an uncompensated attenuator and the response is depending on frequency. To make the response of the attenuator independent of frequency, capacitor C_1 is shunted across R_1. This attenuator now is called a compensated attenuator as shown in.fig.a ,and the same is redrawn as in fig.b

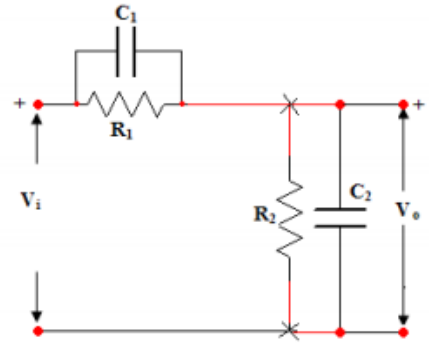


fig.a Compensated Attenuator

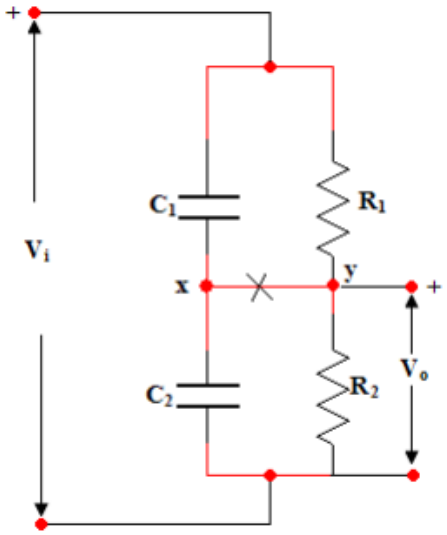
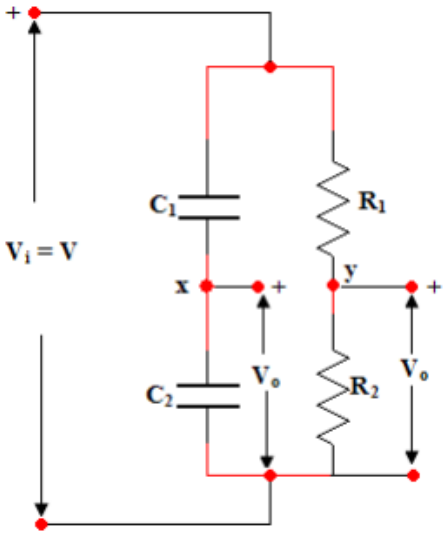


fig.b Compensated attenuator

R_1,R_2,C_1,C_2 form four arms of the bridge. The bridge is said to be balanced when $R_1C_1=R_2C_2$.Then no current flows in the branch xy. Hence for the purpose of computing the output, branch xy is omitted. The resultant circuit is



When a step voltage V_i=V is applied as input, the output is calculated as follows: At t=0+, as the capacitors will not allow any sudden changes in voltage, as the input changes the output also should change abruptly, depending on the values of C_1 and C_2.

$$V(0^+) = V\frac{C_1}{C_1 + C_2}$$

Thus, the initial output voltage is determined by C_1 and C_2.

As $t\to\infty$, the capacitors are fully charged and they behave as open circuits for dc. Hence the resultant output is

$$V_0(\infty) = V\frac{R_2}{R_1 + R_2}$$

Perfect compensation is obtained if, $V_o(0^+)=V_o(\infty)$

i.e. $$\frac{C_1}{C_1 + C_2}V = V\frac{R_2}{R_1 + R_2}$$

From this we get

$C_1R_1=C_2R_2$,or $C_1=(R_2/R_1)C_2=C_p$

and the output is αV_i

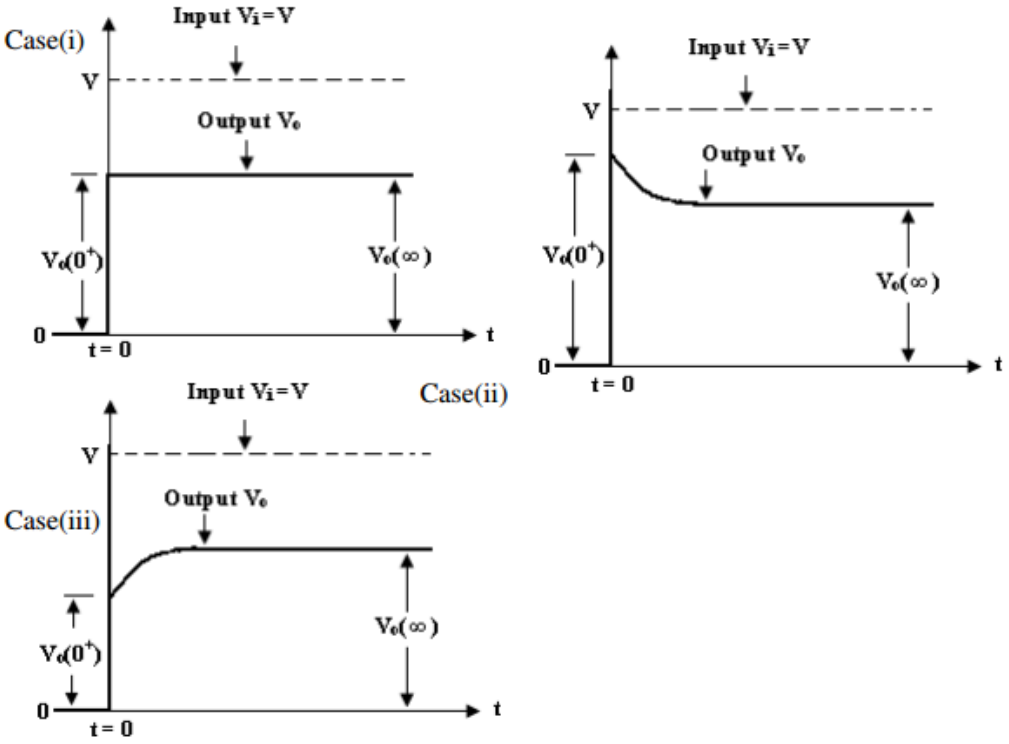
Hence following conditions(cases) arise.

(i) When C_1=Cp, the attenuator is a perfectly compensated attenuator.

(ii) When C_1>Cp , it is an over-compensated attenuator and

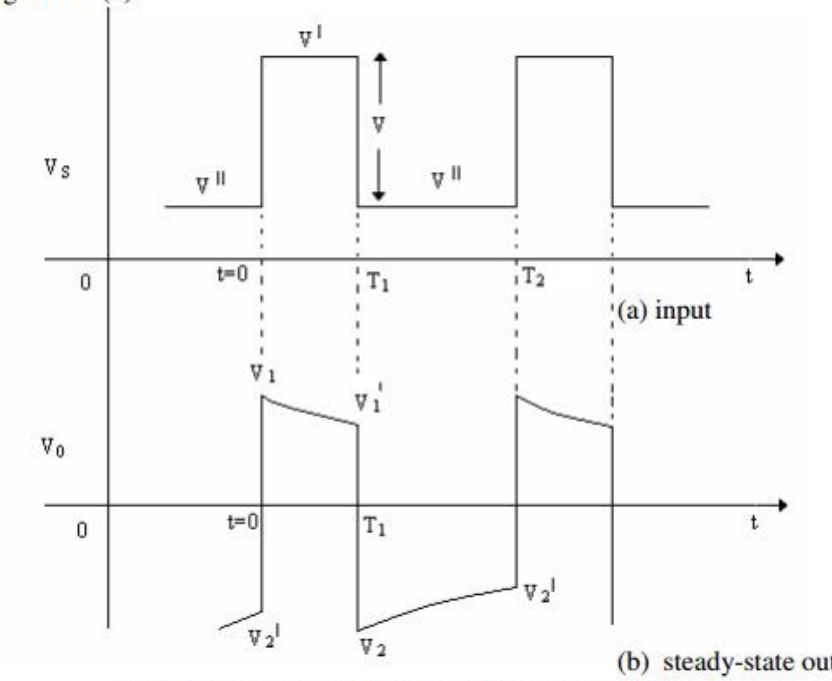
(iii) When C_1<Cp , it is an under-compensated attenuator.

The responses of the attenuator for step input is shown in the following fig.



Practical clamping circuits

If a square wave is applied as input to a clamping circuit, the output reaches the steady-state value after a few cycles. Hence for the input in Fig.(a) the output of the clamping circuit is given in (b).



(b) steady-state output

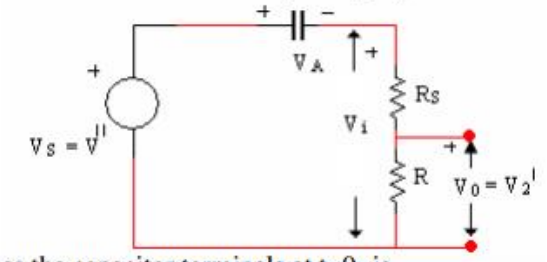
Input and steady-state output of the clamping circuit

The output at steady-state is as in figure above with voltage levels V_1, V_1^1, V_2 and V_2^1. This output can be plotted to scale if the voltages V_1, V_1^1, V_2 and V_2^1 are calculated. To calculate these four unknowns, we need four equations and these four equations are obtained as follows.fig.

(a) consider the situation at t = 0-

At t = 0- , Vs =V^{11} and $V_0 = V_2^1$

The diode is reverse biased and the corresponding equivalent circuit is



The voltage across the capacitor terminals at t=0- is

$V_A(0-) = V_s - V_i$ --------- 2

$V_s = V^{11}$ and $V_2^{1} = V_i \dfrac{R}{R_s + R}$

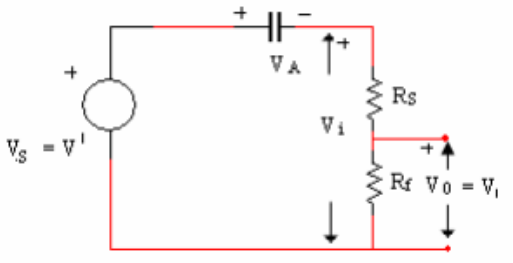
$\therefore V_i = V_2^{1} \dfrac{(R_s + R)}{R}$

Substituting the values of V_s and V_i in equation 2

$\therefore\ V_A(0\text{-}) = V^{11} - V_2^{1} \dfrac{(R_s + R)}{R}$ -------- 3

(b) Consider the situation at the instant t = 0+

At t= 0+, $V_s = V^1$ and $V_0 = V_1$. the diode is ON and the corresponding equivalent circuit is



The voltage across the capacitor terminals at t = 0+ is

$V_A(0+) = V_s - V_i$

$= V^1 - V_i$

$V_1 = V_i \dfrac{R_f}{R_s + R_f}$,

$\therefore\ V_i = \dfrac{(R_s + R_f)}{R_f} V_1$

$\therefore\ V_A(0+) = V^1 - \dfrac{(R_s + R_f)}{R_f} V_1$ -------- 4

Since the voltage across the capacitor cannot change instantaneously

$V_A(0\text{-}) = V_A(0+)$

Hence, from equations 3 and 4

$V^{11} - \dfrac{R + R_s}{R} V_2^{1} = V^1 - V_1 \dfrac{R_s + R_f}{R_f}$ -------- 5

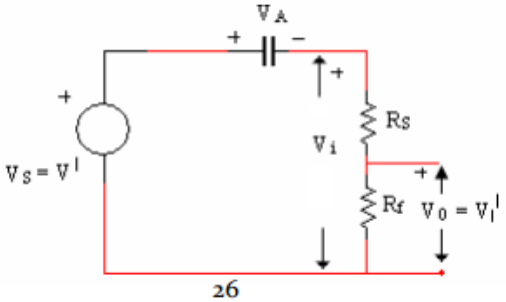
The peak-to-peak amplitude of the input is V. Therefore

$V = V^1 - V^{11}$

From equation 5 ,$V = V^1 - V^{11} = V_1 \dfrac{R_s + R_f}{R_f} - \dfrac{R + R_s}{R} V_2^{1}$ -------- 6

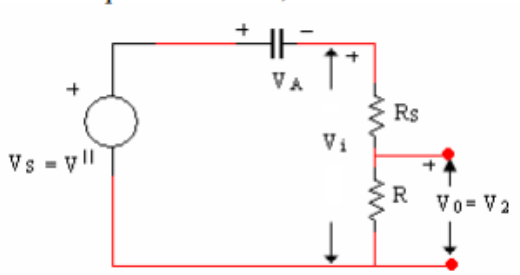
Once again consider the situation at $t = T_1^{-}$, $V_s = V^1$ and $V_0 = V_1^{1}$ and the diode is ON

$V_A(T_1\text{-}) = V_s\text{-}V_i$



$$= V^1 - \frac{R_f + R_s}{R_f} V_1^1 \qquad \text{------- 7}$$

Similarly, at $t = T_1+$ from the equivalent circuit, since D is OFF



$$\therefore V_A(T_1+) = V_s - V_i$$

$$= V^{11} - \frac{R + Rs}{R} V_2 \qquad \text{------- 8}$$

Again as $V_A(T_1-) = V_A(T_1+)$, from equations 7 and 8

$$V^1 - \frac{R_f + R_s}{R_f} V_1^1 = V^{11} - \frac{R + Rs}{R} V_2$$

$$V = V^1 - V^{11} = \frac{R_f + R_s}{R_f} V_1^1 - \frac{R + Rs}{R} V_2 \qquad \text{-------} \qquad 9$$

Further at $t = 0+$, $V_0 = V_1$ and in the interval 0 to T_1, V_0 decays with a time constant $(R_f+R_s)C$

Hence, $V_1^1 = V_1 e^{\frac{-T_1}{(R_f+R_s)C}}$ ---------- 10

Similarly in the interval T_1 to T_2, the diode is reverse biased and the circuit time constant is $(R_s+R)C$

The voltage V_2 decays to V_2^1

$$V_2^1 = V_2 e^{\frac{-(T_2-T_1)}{(R_s+R)C}} \qquad \text{---------} \qquad 11$$

Equations 6, 9, 10 and 11 will enable us to determine the voltage V_1, V_1^1, V_2 and V_2^1. If in the above circuit $R_s = 0$.

Equations 6 and 9 reduce to

$$V = V_1 - V_2^1 = V_1^1 - V_2 \qquad \text{--------} \qquad 12$$

It is evident from the above discussion that the output is independent of the levels V^1 and V^{11} associated with the input and is only determined by the amplitude V.

Subtracting equation 9 from equation 6

$$\frac{R_f + R_s}{R_f}(V_1 - V_1^1) - \frac{R + Rs}{R}(V_2^1 - V_2) = 0 \qquad \text{-------} \qquad 13$$

If $V_1 - V_1^1 = \Delta_f$ and $V_2^1 - V_2 = \Delta_r$

From Equation 13

$$\frac{R_f + R_s}{R_f} \Delta_f = \frac{R + Rs}{R} \Delta_r$$

$$\Delta_f = \frac{R_f}{R_s + R_f} \cdot \frac{R + R_s}{R} \Delta_r$$

If Rs << R

$$\Delta_f = \frac{R_f}{R_s + R_f} \Delta_r \ ,$$

where Δ_f is the tilt in the forward direction and Δ_r is the tilt in the reverse direction .

Let Rs << R_f

Then $\Delta_f \approx \Delta_r$

A clamping circuit that clamps the output to a reference voltage V_R:
The following clamping circuit similar to that we have studied earlier, except for the fact that a reference voltage V_R is included.

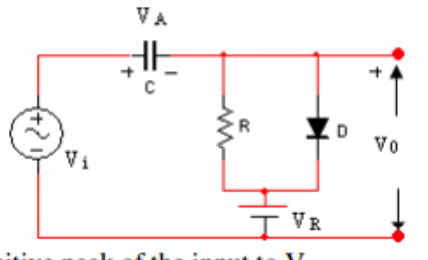
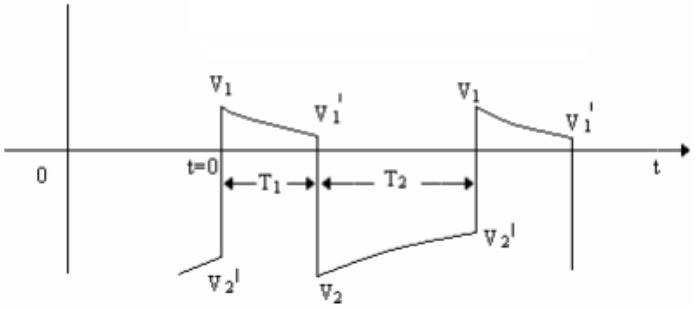


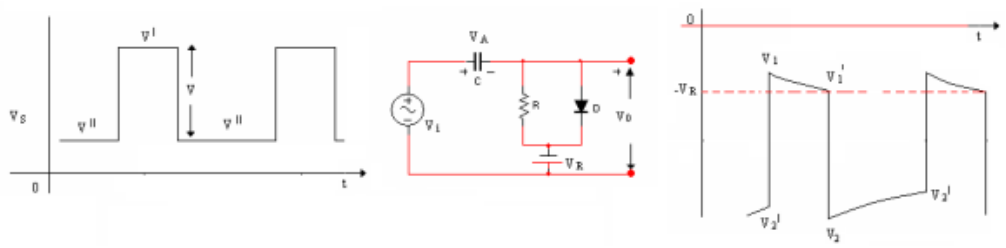
Fig.1 Circuit that clamps the positive peak of the input to V_R

To obtain the steady-state response of the circuit, first assume that V_R is zero. Then this circuit is clamping circuit that clamps the positive peak of the input signal to V_γ.Now the steady-state response for the input of an unsymmetrical square wave, will be as follows.



Solving four equations (we have discussed earlier) the values of V_1, V_1^1, V_2 and V_2^1 can be evaluated. To each of these values calculated add V_R. With the result, the positive peak in the output is clamped to V_R.

If on the other hand, if the polarity of V_R is reversed, add $(-V_R)$ to each of the values computed. The result is that the positive peak in the output is clamped to $(-V_R)$.

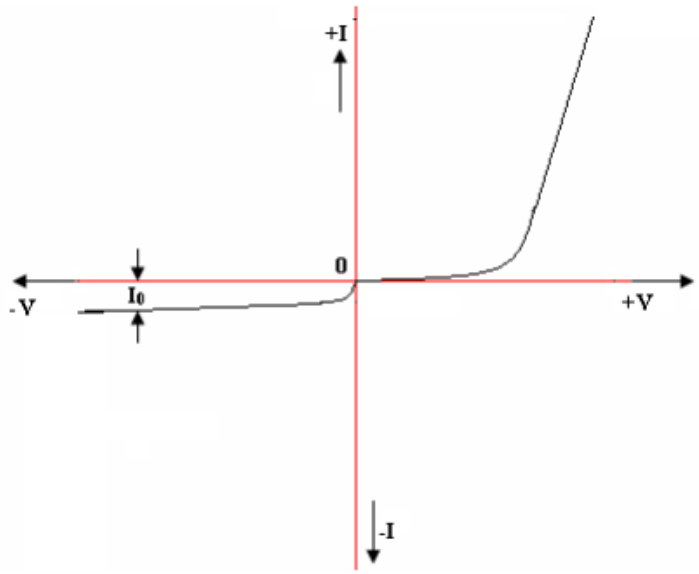


The positive peak of the input clamped to $-V_R$

Switching characteristics of devices

Diode as a switch:

A PN junction diode can be used as a switch. When diode is forward biased, the switch is said to be in the ON state and in reverse-bias, the switch is in the OFF state. The V-I characteristic of a PN junction diode is shown here.



V-I characteristic of a PN diode

The diode current is given by the relation

$$I = I_0 (e^{\frac{V}{\eta V_T}} - 1)$$

where V is the bias voltage, $\eta = 1$ or 2 depending on whether the diode is Ge or Si and V_T is the Volt-equivalent for temperature and at room temperature $V_T = 26mV$.

If $e^{\frac{V}{\eta V_T}} >> 1$, equation 5.1 reduces to

$$I = I_0 e^{\frac{V}{\eta V_T}}$$

When the diode is forward biased V is positive and I is a positive current which varies exponentially with the variation of V. When the diode is reverse-biased V is a negative voltage and the current I now flows in the opposite direction. $I = -I_0$, the reverse saturation current gets doubled for every 10^0C rise in temperature.
When a diode is used as a switch, the device should be ON or OFF depending on the polarity of the signal applied to change state .

Junction diode switching times:

Reverse recovery time of the diode:

Let the diode be ON for some time, as a result there is a large current due to injected hole or electron density.

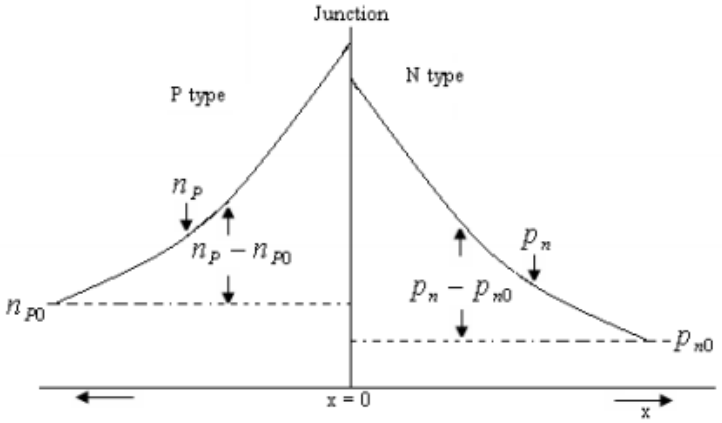


Fig a) Minority carrier density distribution as a function of x, the distance from the junction when the diode is ON

p_{n0} = density of holes on the n-side at equilibrium

n_{P0} = density of electrons on the P-side at equilibrium

n_P = density of electrons on the P-side when forward biased

p_n = density of holes on the n-side when forward biased

$p_n - p_{n0}$ = injected or excess hole density on the n-side

$n_P - n_{P0}$ = injected or excess electron density on the P-side

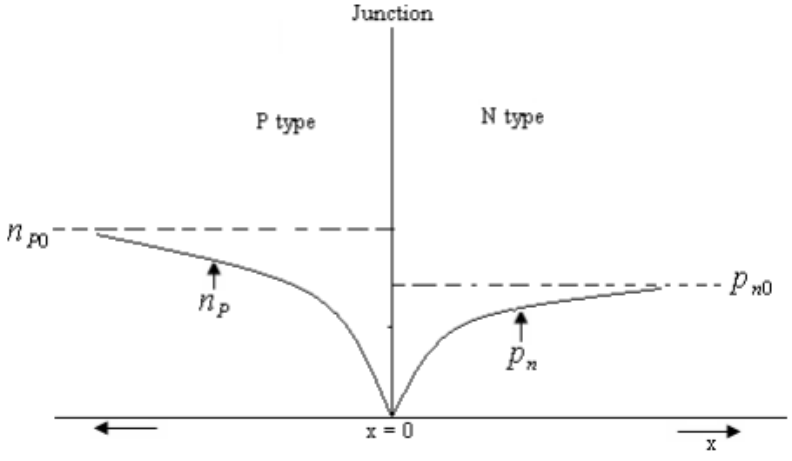
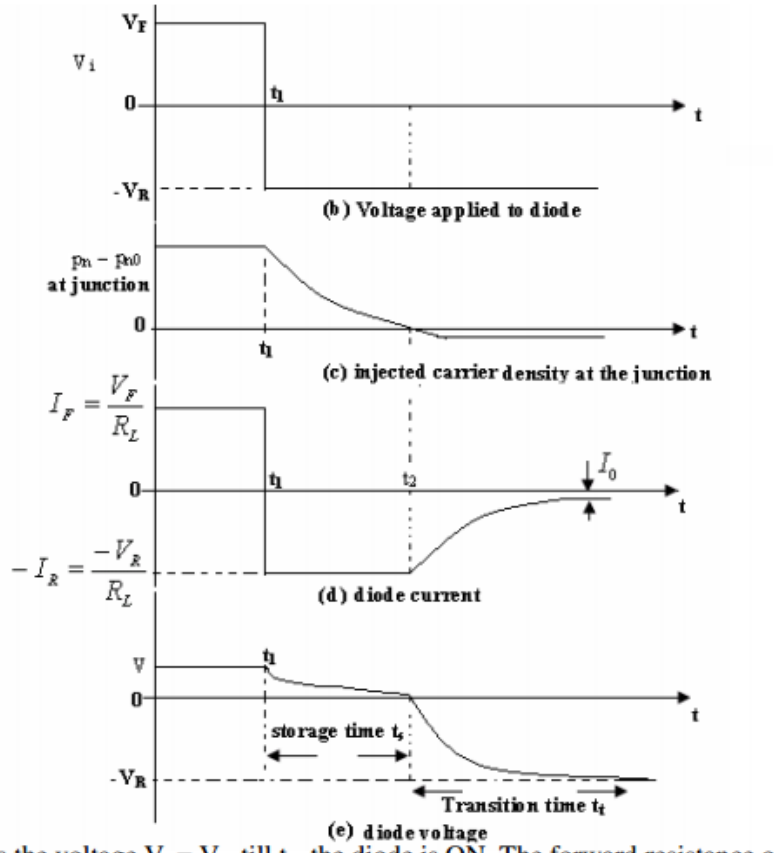


Fig b) Minority carrier density distribution as a function of x, the distance from the junction when the diode is OFF

When the diode is ON the number of minority carriers is large fig(a). When the polarity of the external voltage is suddenly reversed, the diode forward current when ON being large, is to be reduced to reverse current which is very small. But this is not happened as it takes a finite time delay for the minority carrier density distribution to take the form shown in fig.(b). During this period the injected minority carrier density will drop to zero and the minority carrier density reaches the equilibrium value.



As long as the voltage $V_i = V_F$ till t_1, the diode is ON. The forward resistance of the diode being negligible when compared to R_L, therefore $I_F = \frac{V_F}{R_L}$. At $t = t_1$, the polarity of V_i is abruptly reversed, i.e. $V_i = -V_R$ and $-I_R = \frac{-V_R}{R_L}$ until $t = t_2$ at which time minority carrier density p_n at $x = 0$ has reached the equilibrium value p_{n0}.

At $t = t_2$ the charge carriers have been swept, the polarity of the diode voltage reverses, the diode current starts to decrease.

The time duration, t_1 to t_2, during which period the stored minority charge becomes zero is called the **storage time t_s**.

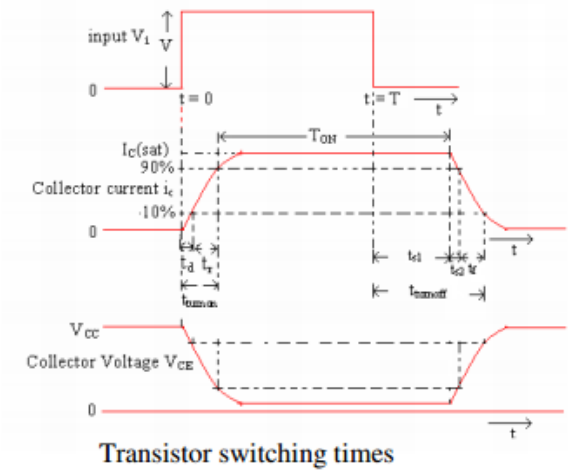
The time interval from t_2 to the instant that the diode has recovered ($V = -V_R$) is called the **transition time,t_t**.

The sum total of the storage time,t_s and the transition time,t_t is called the reverse recovery time of the diode, t_{rr}.

$\therefore \quad t_{rr} = t_s + t_t$

TRANSISTOR SWITCHING TIMES

Let the input to the transistor switch be a pulse of duration T.
When a pulse is applied, because of stray capacitances, collector current will not reach the steady state value instantaneously. To know exactly when the device switches into the ON state and also into the OFF state we define the following switching times of the transistor



Transistor switching times

Delay Time, t_d : It is the time taken for the collector current to reach from its initial value to 10% of its final value
If the rise of the collector current is linear, the time required to rise to 10%I_C(sat) is 1/8 the time required for the current to rise from 10% to 90% I_C(sat).
It is given as

$t_d = \frac{1}{8} t_r$ where t_r is the rise time

Rise Time,t_r : It is the time taken for the collector current to reach from 10% of its final value to 90% of its final value.
However, because of the stored charges, the current remains unaltered for sometime interval t_{s1} and then begins to fall. The time taken for this current to fall from its initial value at t_{s1} to 90% of its initial value is t_{s2}. The sum of these t_{s1} and t_{s2} is approximately t_{s1} and is called the storage time.
Storage time, t_s : It is the time taken for the collector current to fall from its initial value to 90% of its initial value.

Storage time $t_s \cong \tau_s \ln \frac{I_{B1} - I_{B2}}{I_{B\min} - I_{B2}}$

I_{B1} is the base current when the pulse amplitude is V(=12 V) and I_{B2} is the base current when the pulse amplitude is zero.
Fall time, t_f : It is the time taken for the collector current to fall from 90% of its initial value to 10% of its initial value.

Breakdown Voltages:

In a transistor switch, the voltage change which occurs at the collector with switching is nominally equal to the collector supply voltage. Since this voltage change will be used to operate other circuits and devices V_{CC} should be made as large as possible. However, by increasing the value of V_{CC}, the reverse- bias voltage on the collector base diode may become so large that avalanche breakdown may occur in the collector diode. The leakage current I_{C0} will now become MI_{C0} where M is the avalanche multiplication factor. M depends on V_{CB}.

Following empirical relation for M, is considered for many transistor types.

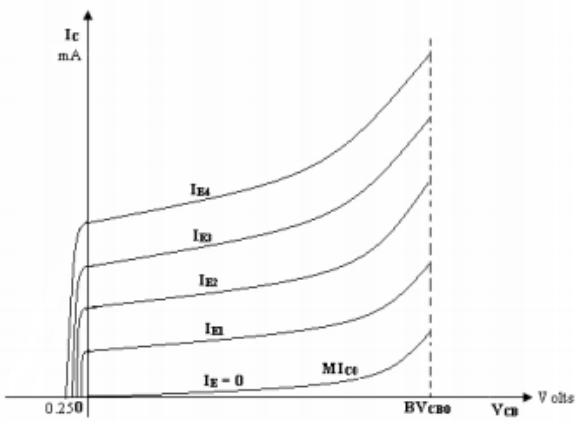
$$M = \frac{1}{1-\left(\frac{V_{CB}}{BV_{CBO}}\right)^n}$$

where BV_{CBO} is maximum reverse bias voltage that can be applied between the collector and base terminals of the transistor when the emitter lead is open circuited .

When n is large, M remains almost approximately at unity till such time V_{CB} reaches BV_{CBO} at which time it becomes infinity abruptly.

On the otherhand, if n is small, the onset of breakdown occurs more gradually.

Let us consider the CB characteristics when extended into the breakdown region.



CB characteristics extended into breakdown region

It is seen from the characteristics, that in the active region, I_C varies slowly and I_C rises sharply as V_{CB} reaches BV_{CBO}.

The current gain in the CB configuration being h_{FB}, the collector current $I_C = h_{FB}I_E$.

Taking the avalanche multiplication into consideration, then

$I_C = Mh_{FB}I_E$

This means that if avalanche multiplication takes place, h_{FB} is seen to have increased by a factor M so that h_{FB}^* in the presence of avalanche multiplication is

$h_{FB}^* = Mh_{FB}$

CE configuration:

It is known that the current gain in CE configuration is h_{FE} and that

$$h_{FE} = \frac{h_{FB}}{1 - h_{FB}}$$

Therefore h_{FE} in the presence of avalanche multiplication is h_{FE}^* and is given by

$$h_{FE}^* = \frac{h_{FB}^*}{1 - h_{FB}^*} = \frac{M\, h_{FB}}{1 - M\, h_{FB}}$$

If $Mh_{FB} = 1$

h_{FE}^* becomes infinity. This means an abruptly large collector current flows when $Mh_{FB} = 1$ which suggests that breakdown has occurred in the device.

From equation

$$M = \frac{1}{h_{FB}}$$

Substituting we have

$$\frac{1}{1 - \left(\frac{V_{CB}}{BV_{CBO}}\right)^n} = \frac{1}{h_{FB}}$$

$$\left(\frac{V_{CB}}{BV_{CBO}}\right)^n = 1 - h_{FB}$$

and $V_{CB} = BV_{CBO} \sqrt[n]{1 - h_{FB}}$

Also $V_{CE} = V_{CB} + V_{BE}$

V_{CB} at breakdown is very much larger than V_{BE}

$\therefore\ V_{CE} \approx V_{CB}$

$$As\ \ \frac{h_{FB}}{1 - h_{FB}} = h_{FE}$$

and as $h_{FB} \approx 1$

$$1 - h_{FB} = \frac{h_{FB}}{h_{FE}} \approx \frac{1}{h_{FE}}$$

From above equations

$$BV_{CEO} = BV_{CBO} \sqrt[n]{\frac{1}{h_{FE}}}$$

If for a transistor, n = 6, $h_{FE} = 50$

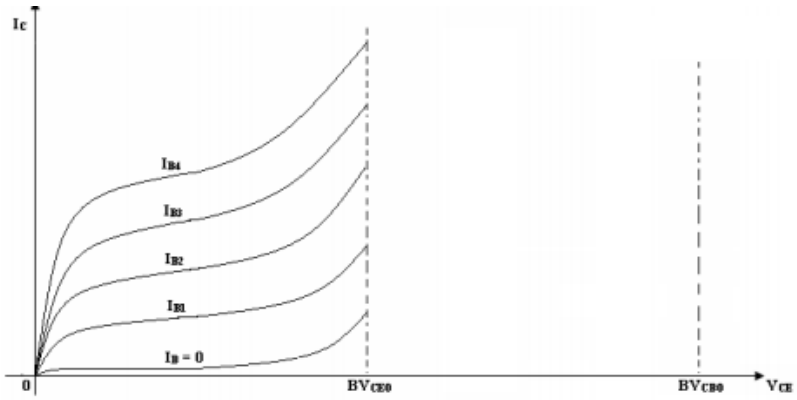
$BV_{CEO} = 0.52 \times BV_{CBO}$

If $BV_{CBO} = 40V$

$BV_{CEO} = 0.52 \times 40 = 20.8V$

BV_{CEO} is approximately half of BV_{CBO}

The CE characteristics extended upto BV_{CEO} are plotted here.



CE characteristics extended up to the breakdown region

MULTIVIBRATORS

Multivibrators are cross-coupled two-stage regenerative amplifiers acting as switching circuits . Multivibrators are broadly classified as

1. Bistable multi or binary or Flip-Flop
2. Monostable multi or One shot multi or univibrator
3. Astble multi or Freerunning multi

Multivibrators are extensively used in digital and switching applications. A bistable multivibrator remains in one of the stable states until we are asked to change. Hence this circuit is essentially used as a memory element in digital circuits..

A monostable multi has only one stable state and one quasi-stable state. Initially the multi is in stable state. After the application of a trigger, the multi goes into the quasistable state and stays there for a finite time and will return back to the initial stable state. Such a circuit is used as a gate.

Other type of multivibrator is an Astable multi which has two quasistable states. This means that change of state occurs in the multi simultaneously. So, the output of this multi is a squarewave. The output of an astable multi is normally used as a clock signal in digital circuits.

BISTABLE MULTIVIBRATORS

Introduction:

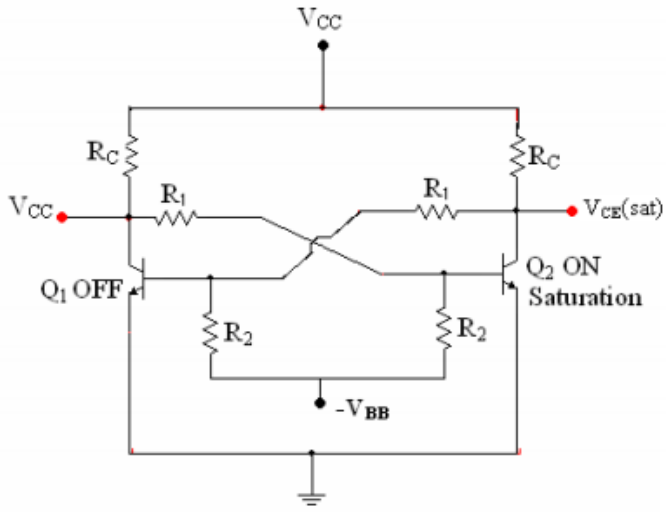
. This circuit has two devices Q_1 and Q_2. Let initially be Q_1 , OFF and Q_2 , ON . On the application of a trigger Q_1 goes to ON and Q_2 goes to OFF . When next trigger is applied Q_1 goes OFF and Q_2 goes ON. If the ON device is driven in to saturation, the Binary is called saturating Binary. If on the otherhand, the ON device is held in the active region, the binary is called a non-saturating binary.

Consider two types of Bistable multivibrator circuits.

1. Fixed bias binary
2. Self bias binary

Fixed bias binary:

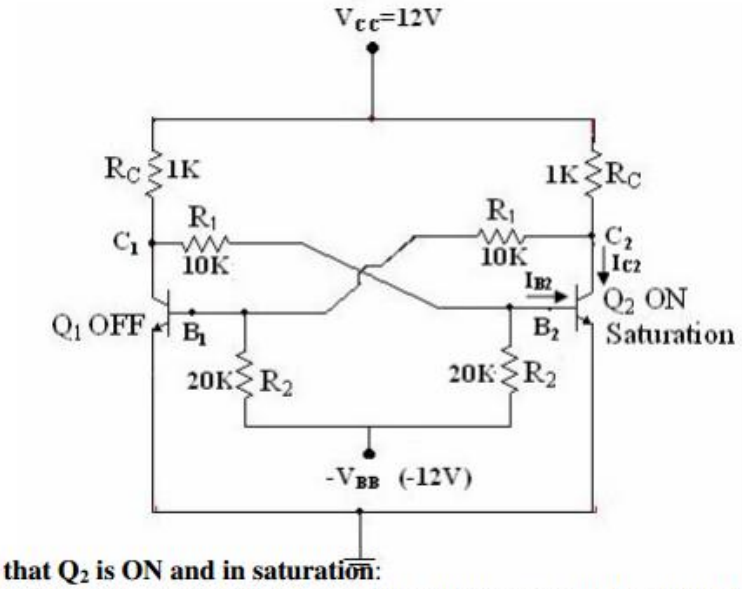
The circuit shown in fig.below is a fixed-bias binary



Let initially Q_1 be OFF and Q_2 be in ON. Then the voltage at the first collector is V_{CC} and the voltage at the second collector is $V_{CE}(sat)$. If a negative trigger is applied at the base of the ON device (Q_2), Q_2 goes into the OFF i.e. its collector voltage rises to V_{CC} . Consequently Q_1 goes into the ON state and its collector voltage falls to $V_{CE}(sat)$.

PROBLEM ON FIXED BIAS

To verify whether Q_1 is really OFF and Q_2 is really ON and in saturation, consider the following circuit.This circuit uses npn silicon transistors having h_{FEmin} = 50, $V_{CE}(sat)$=0.3V, $V_{BE}(sat)$= 0.7V, V_{CC}=12V, V_{BB}=12V, R_C=1K, R_1=10K, R_2=20K



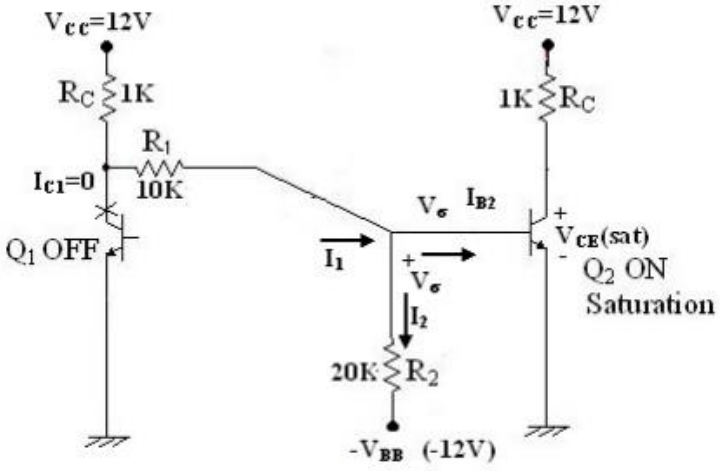
To verify that Q_2 is ON and in saturation:

To verify this, base current I_{B2} and its collector current I_{C2} should be calculated. If the base current calculated is much in excess of the minimum base current then Q_2 is really in saturation.

To verify Q_1 is in OFF :

The transistor Q_1 is OFF if its base–emitter junction is reverse biased. For this , the voltage at the base of Q_1 is to be calculated. If it reverse biases the emitter junction, then the transistor Q_1 is indeed in the OFF state.

To calculate I_{B2}: Consider the part of the circuit.



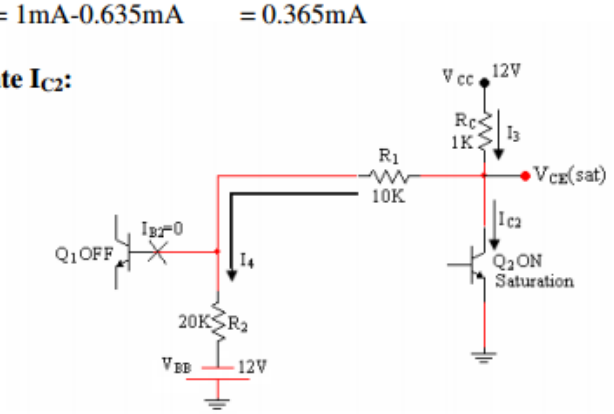
Taking the assumption that Q_2 is in saturation and Q_1 is OFF, calculate I_1 and I_2 to determine I_{B2}. Then $I_{B2} = I_1 - I_2$

$$I_1 = \frac{V_{CC} - V_\sigma}{R_C + R_1} = \frac{12 - 0.7}{1 + 10} = \frac{11.3V}{11K} = 1mA$$

$$I_2 = \frac{V_\sigma - (-V_{BB})}{R_2} = \frac{12.7}{20K} = 0.635mA$$

$I_{B2} = I_1 - I_2 = 1\text{mA} - 0.635\text{mA} = 0.365\text{mA}$

To calculate I_{C2}:



$$I_3 = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{12 - 0.3}{1K} = 11.7mA$$

$$I_4 = \frac{V_{CE(sat)} - (-V_{BB})}{R_1 + R_2} = \frac{12 + 0.3}{30K} = \frac{12.3}{30K} = 0.41mA$$

$I_{C2} = I_3 - I_4 = 11.7 - 0.41$

$= 11.29\text{mA}$

To verify Q_2 is in saturation:

$$I_{B2\min} = \frac{I_{C2}}{h_{FE\min}} = \frac{11.29mA}{50} = 0.226mA$$

For Q_2 to be in saturation

$I_{B2} \cong 1.5 I_{B2\min}$

$$I_{B2} = 1.5 \times 0.226mA = 0.339mA$$

i.e. $I_{B2} >> I_{B2(min)}$

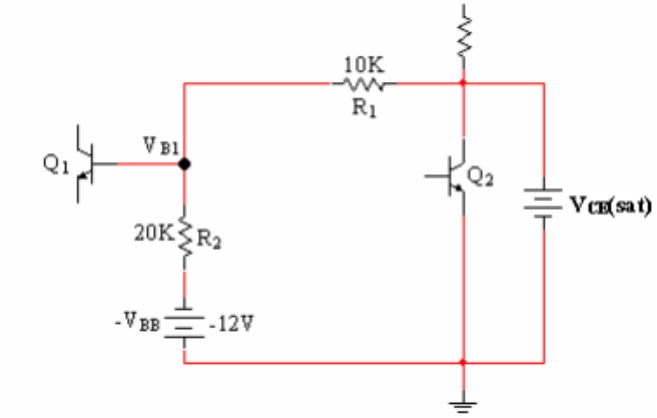
Actually $I_{B2} = 0.365$mA.

Hence Q_2 is really in the saturation.

Hence $V_{C2} = 0.3$V, $V_{B2} = 0.7$V

To verify that Q_1 is OFF :

To Calculate V_{B1}, consider other part of the circuit.



The voltage V_{B1} at the base of Q_1 is due to two sources, $-V_{BB}$ source and $V_{CE}(sat)$ source. Using the superposition theorem

$$V_{B1} = V_{CE(sat)} \frac{R_2}{R_1 + R_2} + (-V_{BB}) \frac{R_1}{R_1 + R_2}$$

$$= 0.3 \times \frac{20}{30} - 12 \times \frac{10}{30}$$

$$= 0.2\text{-}4$$

$$= -3.8\text{V}.$$

This voltage reverse-biases the emitter junction of Q_1 . Hence Q_1 is OFF.

Therefore $V_{C1} = V_{CC} = 12$V

But V_{C1} is not exactly 12V as it should be when Q_1 is OFF, but is smaller than this because of the cross-coupling network. The actual voltage at the first collector is

$V_{C1} = V_{CC} - I_1 R_C$

$= 12 - (1\text{mA})\ (1\text{K}) = 11$V

Hence the voltages in the initial stable state are

$V_{C1} = 11$V, $V_{B1} = -3.8$V, $V_{C2} = 0.3$V, $V_{B2} = 0.7$V

Design of a fixed bias binary :

Design a fixed bias binary with supply voltages ±12V, NPN silicon devices having $V_{CE}(sat)= 0.2V$, $V_{BE}(sat)=V_\sigma = 0.7V$ and $h_{FEmin}=50$ are used.
Assume $I_C = 5mA$.

$$R_C = \frac{V_{CC} - V_{CE(sat)}}{I_{C2}} = \frac{12 - 0.2V}{5mA} = \frac{11.8V}{5mA}$$

$$= 2.36K\Omega$$

$\approx$ 2.2K (standard resistance)

$$R_2 = \frac{V_\sigma - (-V_{BB})}{I_2}$$

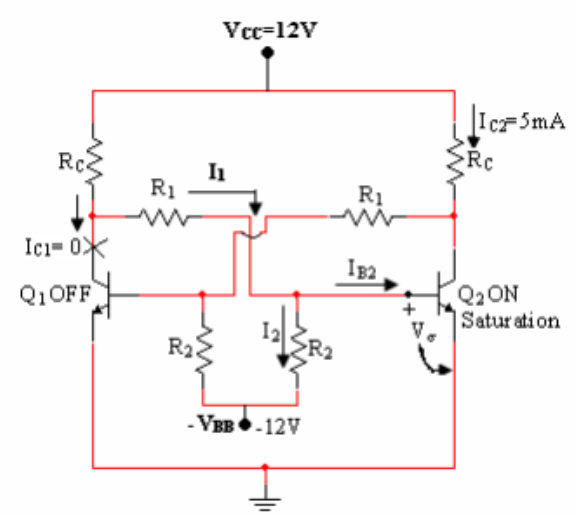
$$Choose \quad I_2 \approx \frac{1}{10} I_{C2}$$

$$= 0.5mA$$

$$\therefore R_2 = \frac{0.7 + 12}{0.5} = \frac{12.7V}{0.5mA} = 25.4K\Omega$$

$$\approx 22K\Omega$$

$$I_{B2\,min} = \frac{I_{C2}}{h_{FE\,min}} = \frac{5mA}{50} = 0.1mA$$



If Q_2 is in saturation

$$I_{B2} = 1.5 I_{B2\,min}$$

$$= 0.15mA$$

$$I_1 = I_2 + I_{B2}$$

$$= 0.5mA + 0.15mA = 0.65mA$$

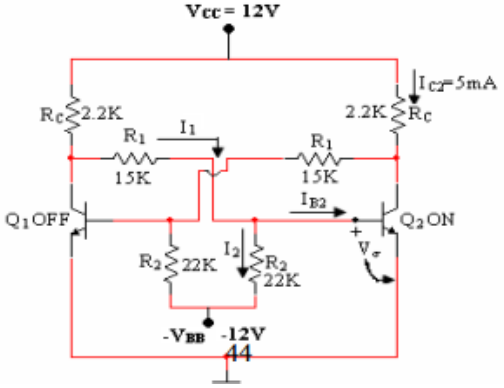
$$R_C + R_1 = \frac{V_{CC} - V_\sigma}{I_1} = \frac{12 - 0.7}{0.65mA} = \frac{11.3V}{0.65mA} = 17.38K\Omega$$

$$R_1 = (R_C + R_1) - R_C$$

$$= 17.38 - 2.36 = 15.02K\Omega$$

$$Choose \quad R_1 = 15K\Omega$$

The circuit, so designed, with component values indicated is shown below:



After the design is complete, verify whether Q_2 is in saturation and Q_1 is OFF or not.

$$I_{C2} \approx \frac{V_{CC} - V_{CE}(sat)}{2.2K}$$

$$= \frac{12 - 0.2V}{2.2K} = \frac{11.8V}{2.2K} = 5.36mA$$

$$I_{B2\min} = \frac{5.36mA}{50} = 0.107mA$$

$$I_2 = \frac{V_\sigma + V_{BB}}{R_2} = \frac{12.7}{22K} = 0.58mA$$

$$I_1 = \frac{V_{CC} - V_\sigma}{R_C + R_1}$$

$$= \frac{12 - 0.7}{2 + 10}$$

$$= \frac{11.3}{12}$$

$$= 0.94mA$$

$$I_{B2} = I_1 - I_2$$

$$= 0.94mA - 0.58mA$$

$$= 0.36mA$$

$$I_{B2} \geq I_{B2\min}$$

Hence Q_2 is in saturation

$$V_{B1} = V_{CE}(sat)\frac{R_2}{R_1 + R_2} - V_{BB}\frac{R_1}{R_1 + R_2}$$

$$= 0.2 \times \frac{22}{10 + 22} - 12 \times \frac{10}{10 + 22}$$

$$= 0.137 - 3.75$$

$$= -3.613V$$

Hence Q_1 is OFF

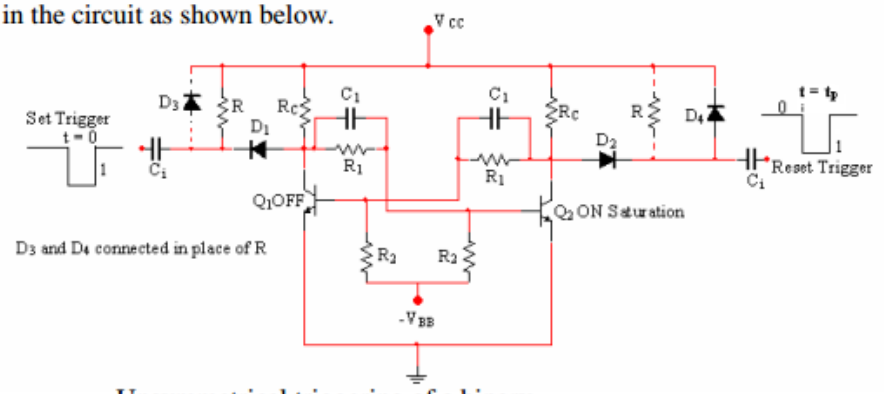
Methods of triggering a binary:

To change the binary from one stable state to the other, a pulse of short duration with sufficient amplitude (called trigger) of proper polarity should be applied at the input(output) of an active device the circuit. The trigger can be a dc trigger or it can be a pulse trigger. There are two triggering methods to change the state of multivibrator.

1. Unsymmetrical triggering
2. Symmetrical triggering.

Unsymmetrical triggering:

In unsymmetrical triggering, one trigger pulse, taken from a source, is applied at one point in the circuit. The next trigger pulse taken from a different source is applied at a different point in the circuit as shown below.



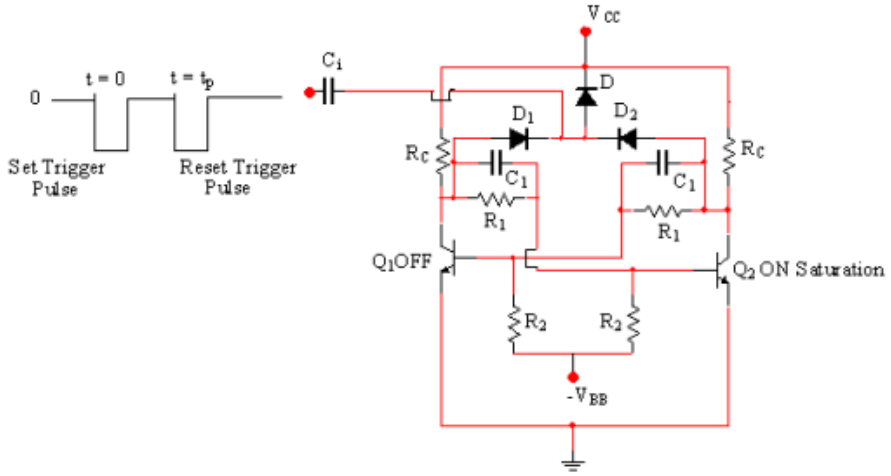
Unsymmetrical triggering of a binary

Let the trigger be applied to the collector C_1 of the circuit at t=0. If Q_1 is OFF, D_1 is ON and this negative pulse appears at the base of Q_2 as the first collector and second base are connected. Q_2 goes into the OFF state and Q_1 into the ON state.The next through C_1 trigger pulse, i.e. the Reset pulse, is applied through D_2 at the second collector C_2 which is coupled to the first base through C_1. Q_1 now goes into the OFF state and Q_2 into the ON state. Unsymmetrical triggering is used to generate a gated output, the width of this gate must be at least equal to the spacing between two successive triggers.

To prevent the loading down problem from the trigger source , R should be large. But when a trigger is applied, a charge is built up on the condenser C_i. If the charge is to be quickly removed before the application of the next trigger signal at this terminal, R should be small. So while choosing the value of resistance R a compromise is necessary. A single resistance cannot simultaneously satisfy these two requirements. Hence in place of R, diodes D_3 and D_4 are used. When a pulse appears, the diode is OFF (D_3 or D_4), a large reverse resistance of the diode appears in place of R. Otherwise the diode is ON offering negligible resistance so that the charge on the capacitance can be quickly removed.

Symmetrical triggering:

In symmetrical triggering, one triggering pulse generator is taken to change from one stable state to the other in one direction. The same is used to change the state in reverse direction also. This method of triggering is normally used in counters.

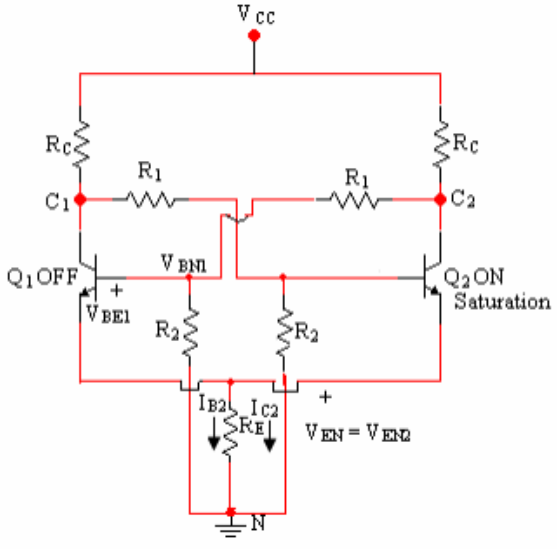


Symmetric triggering of binary

The purpose of D is similar to the diodes D_3 and D_4 used earlier. The first trigger pulse makes D_1 conduct and this pulse is coupled to the base of Q_2 and drives Q_2 into the OFF state and Q_1 into the ON state. The next trigger pulse applied at $t = t_p$ is coupled to the base of Q_1 as D_2 is now ON. Hence Q_1 again goes into the OFF state and Q_2 into the ON state. D_1 and D_2 are called steering diodes as these diodes steer the trigger pulse train.

Self-bias binary :

In a fixed bias binary there are two separate sources, V_{CC} and V_{BB}. Instead two we can design a binary with one power supply using self-bias method.



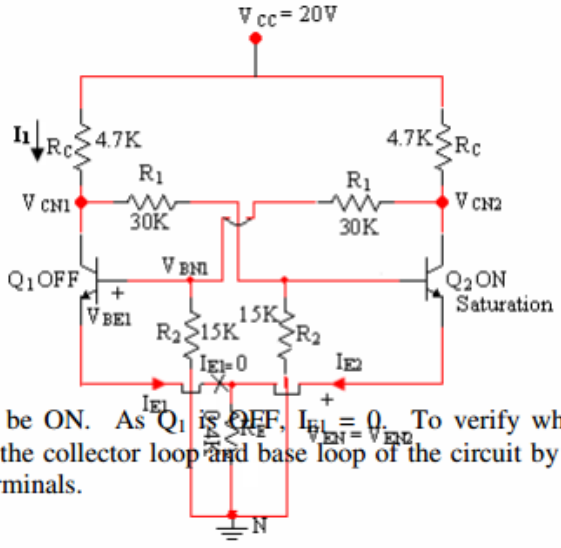
Self-bias Binary

Let Q_2 be ON and in saturation, in the initial stable state. As a result I_{B2} and I_{C2} flow through R_E developing a voltage V_{EN}. The voltage between the base emitter terminals of Q_1 is V_{BE1} and it is $V_{BE1} = V_{BN1} - V_{EN}$

If this voltage reverse biases the emitter diode of Q_1, then Q_1 is indeed in the OFF state.

To calculate the stable state currents and voltages consider a practical circuit.

In npn silicon transistors are used. $V_{BE}(sat) = 0.7V$, $V_{CE}(sat) = 0.4V$ and $h_{FEmin} = 50$, $V_{CC} = 20V$, $R_C = 6.7K$, $R_1 = 30K$ and $R_2 = 15K$, $R_E = 400\Omega$



Let Q_1 be OFF and Q_2 be ON. As Q_1 is OFF, $I_{E1} = 0$. To verify whether Q_2 is in saturation or not , draw the collector loop and base loop of the circuit by thevenising at the collector and base terminals.

$$V_{thb} = V_{CC} \times \frac{R_2}{R_C + R_1 + R_2}$$

$$= 20 \times \frac{15}{4.7 + 30 + 15}$$

$$= 6.03V$$

and

$$R_{thb}=R_2//(R_C+R_1) = \frac{R_2(R_C + R_1)}{R_2 + R_C + R_1}$$

$$= \frac{(15)(30+4.7)}{4.7+30+15}$$

$$=10.47K$$

$$V_{thc} = V_{CC} \times \frac{(R_1 + R_2)}{R_C + R_1 + R_2}$$

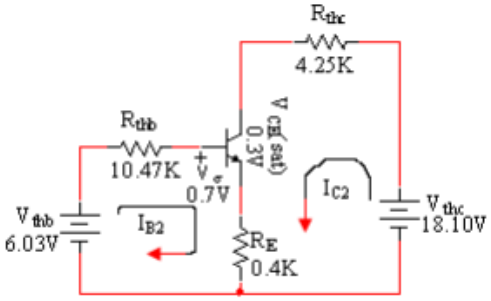
$$= \frac{20 \times (30+15)}{4.7 + 30 + 15}$$

$$= 18.10V$$

$$R_{thc} = (R_1 + R_2) // R_C$$

$$= \frac{(30+15)(4.7)}{30+15+4.7}$$

$$= 4.25K$$



Using KVL at the input and output loops

$6.03-0.7 = (10.47+0.4)\ I_{B2}+0.4I_{C2}$ ---------- (1)
$18.10-0.3 = 0.4I_{B2}+ (6.25+0.4)\ I_{C2}$ ---------- (2)
i.e.
$5.33V=10.87I_{B2}+0.4I_{C2}$
$17.80V=0.4I_{B2}+6.65I_{C2}$
From which

I_{B2}=0.35mA
I_{C2}=3.79mA

$$I_{B2\min} = \frac{I_{C2}}{h_{FE}} = \frac{3.79mA}{50}$$

$$= 0.076mA$$

$$I_{B2} >> I_{B2\min}$$

Hence Q_2 is saturation

$$\therefore V_{EN} = V_{EN2} = (I_{B2} + I_{C2})R_E$$

$$V_{CN2} = V_{EN2} + V_{CE(sat)}$$

$$= (1.66V + 0.4V) = 2.06V$$

$$V_{BN2} = V_{EN2} + V_{\sigma}$$

$$= (1.66V + 0.7V) = 2.36V$$

$$V_{BN1} = V_{CN2} \times \frac{R_2}{R_1 + R_2}$$

$$= \frac{2.06 \times 15}{15 + 30}$$

$$= 0.69V$$

$$V_{BE1} = V_{BN1} - V_{EN2}$$

$$= (0.69V - 1.66) = -0.97V$$

As this voltage reverse biases the emitter diode, Q_1 is OFF.

$$I_1 = \frac{V_{CC} - V_{BN2}}{R_C + R_1}$$

$$= \frac{20 - 2.36}{4.7 + 30}$$

$$= 0.51mA$$

$$V_{CN1} = V_{CC} - I_1 R_C$$

$$= 20 - (0.51)(4.7)$$

$$= 17.6V$$

The stable state voltages are

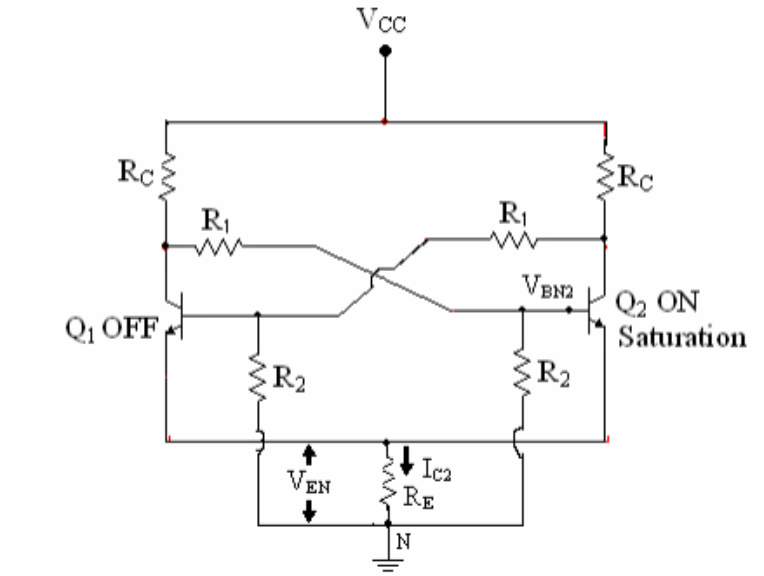
V_{CN1}=17.6V, V_{BN1}=0.69V

V_{CN2}=2.06V V_{BN2}=2.36V

V_{EN}=1.66V

Design of a self-bias binary :

Design a self-bias binary using silicon npn transistors whose junction voltages are $V_{CE}(sat) = 0.3V$, $V_{BE}(sat) = 0.7V$, $V_{BE}(cut\text{-}off) = 0V$, $h_{FEmin} = 50$, $V_{CC} = 9V$, $I_C = 4mA$.



Solution:

Assume $V_{EN}=\frac{1}{3}V_{CC}=\frac{1}{3}\times 9=3V$

and I_{C2} =4mA

$$I_{B2min}=\frac{4mA}{50}=0.08mA$$

Choose $I_{B2} = 1.5I_{B2min}$=0.12mA

$(I_{C2}+I_{B2}) = 4+0.12 = 4.12$mA

$$R_E=\frac{V_{EN2}}{I_{C2}+I_{B2}}=\frac{3V}{4.12mA}=0.728K\Omega$$

Select $R_E \approx 500\,\Omega$

$$R_C=\frac{V_{CC}-V_{CE}(sat)-V_{EN2}}{I_C}$$

$$=\frac{9-0.3-3}{4mA}=\frac{5.7V}{4mA}=1.425K\Omega$$

Choose R_C=1K

Let

$$I_2 = \frac{1}{10} I_{C2} = \frac{1}{10} \times 4mA = 0.4mA$$

$$V_{BN2} = V_{EN2} + V_\sigma = 3 + 0.7 = 3.7V$$

$$R_2 = \frac{V_{BN2}}{I_2} = \frac{3.7V}{0.4mA} = 9.25K$$

Choose $R_2 = 10K$

Find I_2 for this R_2

$$I_2 = \frac{V_{BN2}}{R_2} = \frac{3.7V}{10K} = 0.37mA$$

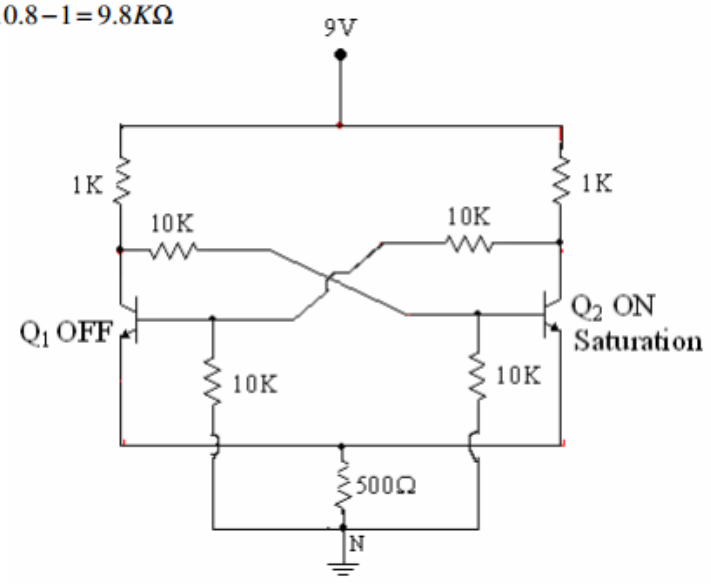
$$R_C + R_1 = \frac{V_{CC} - V_{BN2}}{I_2 + I_{B2}}$$

$$= \frac{9 - 3.7}{0.37 + 0.12} = \frac{5.3V}{0.49mA} = 10.8K\Omega$$

$$(R_C + R_1) = 10.8K\Omega$$

$$(R_C + R_1) - R_C = 10.8 - 1 = 9.8K\Omega$$

Choose $R_1 = 10K$



Having fixed the component values, once again verify whether Q_2 is really in saturation or not and Q_1 is OFF or not.

When calculated

I_{B2}=0.149mA, I_{C2}=5.46mA, I_{B2min}=0.109mA, V_{EN2}=2.8V, V_{CN2}=3.1V, V_{BN1}=1.55V, $V_{BE1}=V_{BN1}-V_{EN2}$= -1.25V

These values show that Q_1 is OFF and Q_2 is in saturation

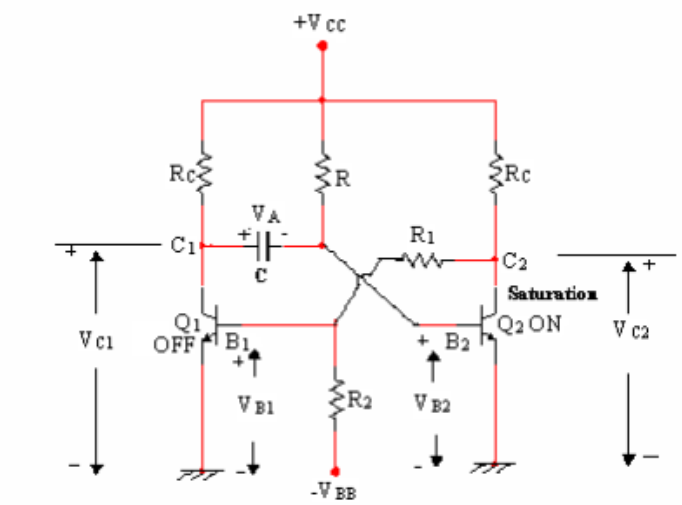
Monostable Multivibrator

Introduction:

This circuit consists of two active devices Q_1 and Q_2, one is in the OFF state, say (Q_1) and the other, Q_2 in the ON state. These devices remain in the same state forever. Only on the application of a trigger, the multi goes into the quasistable state (Q_1 ON and Q_2 OFF) and after a time interval T, will return to the stable state (Q_1 OFF and Q_2 ON). Thus this circuit generates a gate pulse of duration T.

The output of this circuit is high for a time duration T called the pulse duration, pulse width or gate width.

Collector-Coupled monostable multi: The collector coupled monostable multivibrator is shown below.



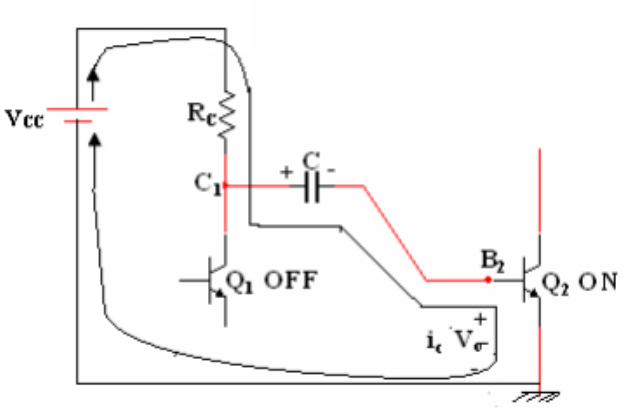
Collector-coupled monostable multi

In the stable state Q_1 is OFF and Q_2 is ON . Therefore

$V_{C1} = V_{CC}$

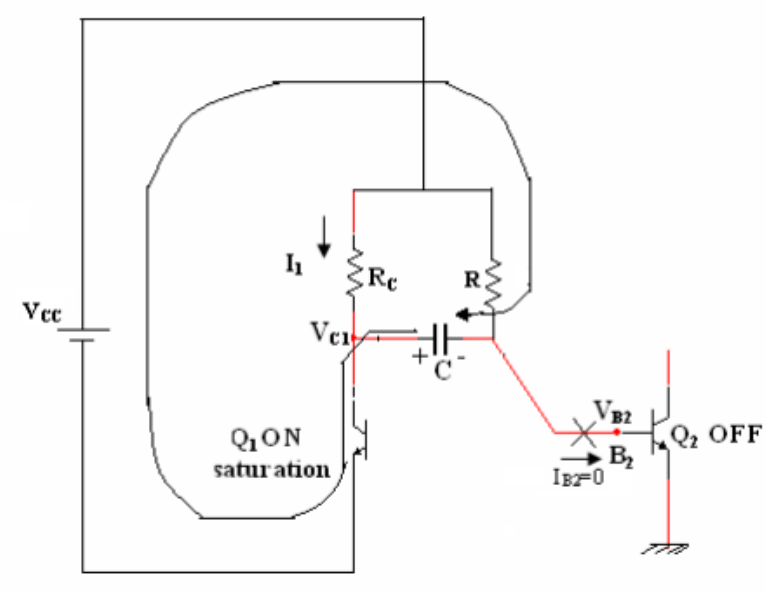
$V_{C2} = V_{CE}(sat)$

$V_{B2}=V_{BE}(sat)=V_{\sigma}$



Charging of C

C now tries to charge to V_{CC} through R_C of Q_1 and small input resistance of Q_2,. As $t \rightarrow \infty$, this voltage reaches V_{CC}. On the application of a trigger at t=0, (a negative pulse at B_2), Q_2 goes into the OFF state and Q_1 is driven into the ON state and preferably into saturation. Hence there is a current I_1 in Q_1. V_{C1} is $V_{CE}(sat)$, if $I_1=I_C(sat)$



Q_1 is ON in the quasistable state

The charge on C now discharges with a time constant τ=RC,. As a result the voltage at B_2 changes as a function of time .When this voltage V_{B2} at B_2 reaches V_γ after a time interval T, Q_2 is switched ON and Q_1 is switched OFF due to regeneration, thus ending the quasistable state.

The voltage variation at B_2 of Q_2

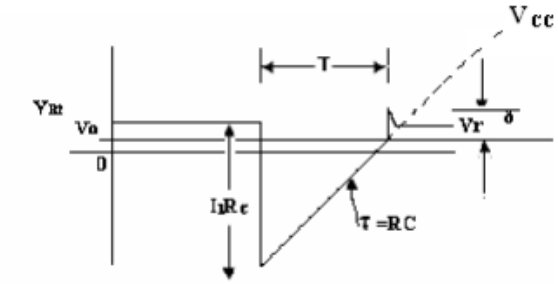


Fig.7.5. Voltage variation at the base of Q_2 in the quasistable state.

The time period T can be calculated as T= 0.69RC, if Q_1 in the quasistable state is in saturation, since $I_1R_C = V_{CC}-V_{CE}(sat)$

Gatewidth of a collector coupled mono stable:

A monostable multi can be used as a voltage to time converter as shown in Fig

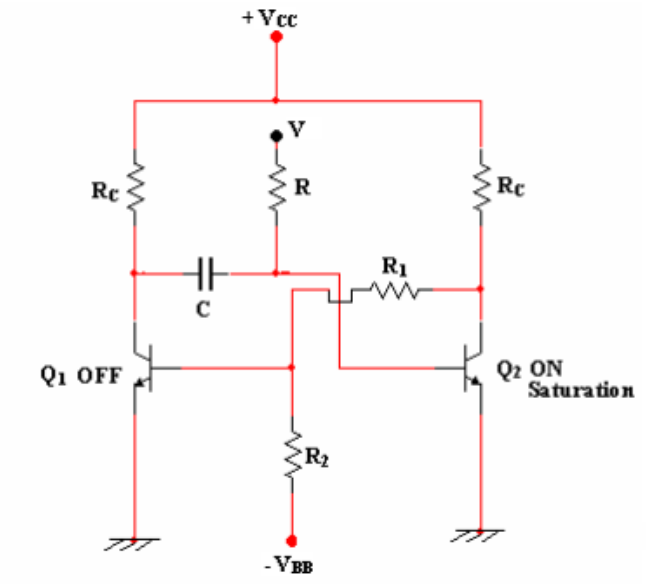


Fig. . Monostable as a voltage to time converter

The time T for which Q_1, in the quasistable state, is ON and Q_2 is OFF is calculated. Consider the voltage variations at B_2, fig.7.17

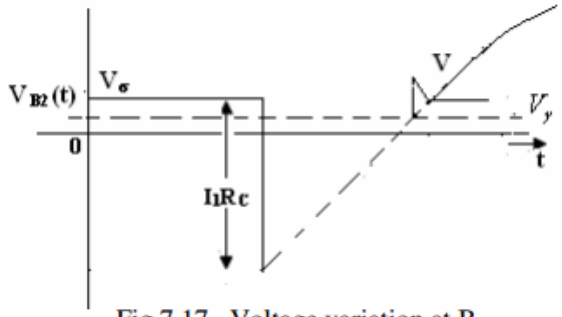


Fig.7.17 Voltage variation at B_2

$V_{B2}(t) = V_f - (V_f - V_i)e^{\frac{-t}{\tau}}$

$V_f = V$

$V_i = V_\sigma - I_1R_C$

If Q_1 is in saturation

$I_1R_C = V_{CC} - V_{CE}(sat)$

$V_i = V_\sigma - V_{CC} + V_{CE}(sat)$

$$V_{B2}(t) = V - (V - V_{\sigma} + V_{CC} - V_{CE}(sat))e^{\frac{-t}{\tau}}$$

At t = T

$V_{B2}(t) = V_{\gamma}$

$$V_{\gamma} = V - (V - V_{\sigma} + V_{CC} - V_{CE}(sat)e^{\frac{-T}{\tau}}$$

As V_{γ}, V_{σ} and $V_{CE}(sat)$ are small when compared to V and V_{CC}

$$\therefore \quad 0 = V - (V + V_{CC})e^{-\frac{T}{\tau}}$$

$$T = \tau \ln \frac{(V + V_{CC})}{V}$$

$$T = \tau \ln(1 + \frac{V_{CC}}{V})$$

Thus, to change T, V can be varied.

ASTABLE MULTIVIBRATOR

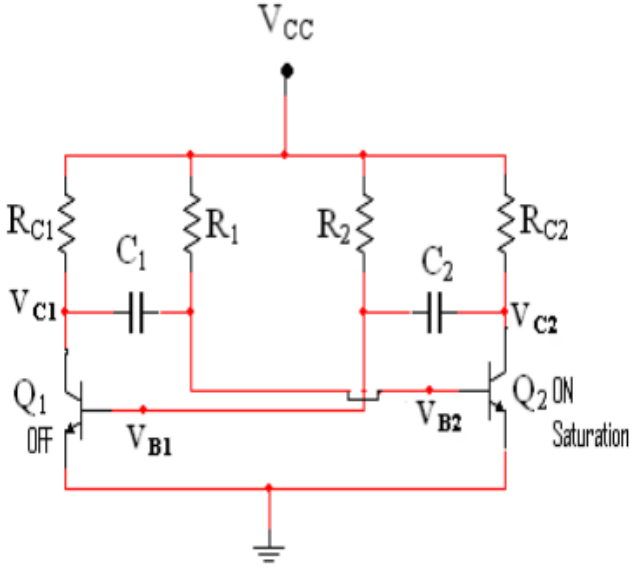
Introduction:

Two cross-coupled switching circuits are connected in this arrangement. The devices in this Multivibrator will not remain in one state (either ON or OFF) forever. Change of state in the devices occurs continuously after a finite time interval depending on the circuit components used. Hence this circuit has two quasistable states.

Let Q_1 and Q_2 be two transistors used. If Q_1 is ON, then Q_2 is OFF. These will remain in this state only for a fixed time duration after which Q_1 switches into the OFF state and Q_2 into the ON state without applying triggering pulse and this process is repeated. Therefore it is also called Free running multivibrator. The output of the circuit is a squarewave, having two time periods,T_1 and T_2. If $T_1 = T_2=T/2$, then the circuit is a symmetric astable multivibrator. If $T_1 \neq T_2$, then it is called an unsymmetrical astable multi-vibrator. The astable multivibrator is essentially a squarewave generator.

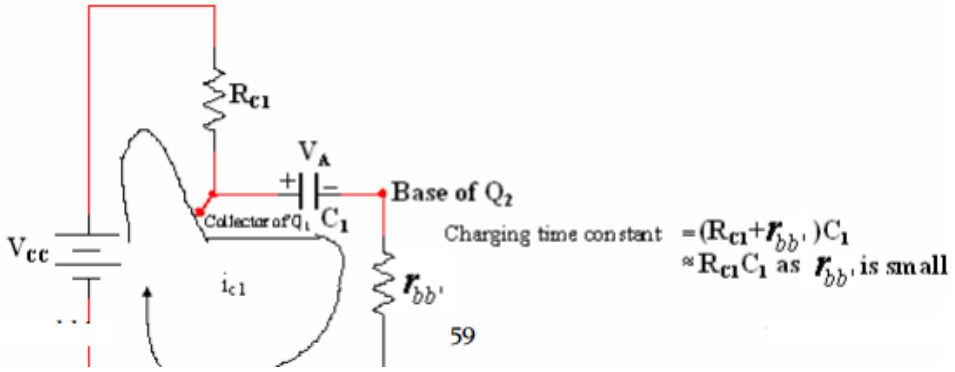
Collector Coupled astable multi:

Collector coupled astable multi is shown below.



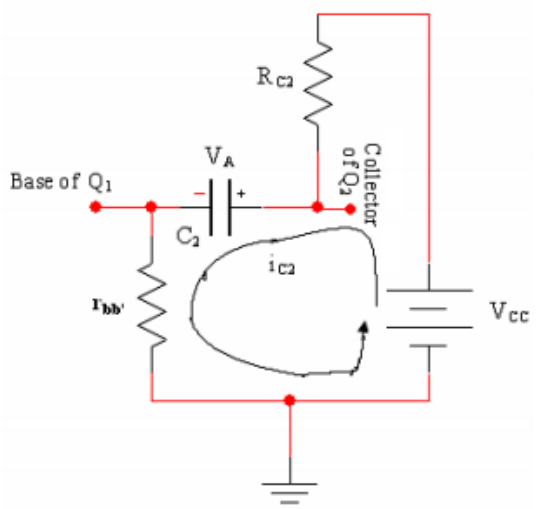
astable multi

Assume that transistor Q_1 is OFF and Q_2 is ON initially. Then $V_{B2} = V_\sigma$, $V_{C2} = V_{CE}(sat)$ and $V_{C1}=V_{CC}$. With Q_1 OFF and Q_2 ON, C_1 will try to charge to the supply voltage through the collector resistance R_{C1} and through the base and emitter terminals of Q_2.



Charging of capacitor C_1

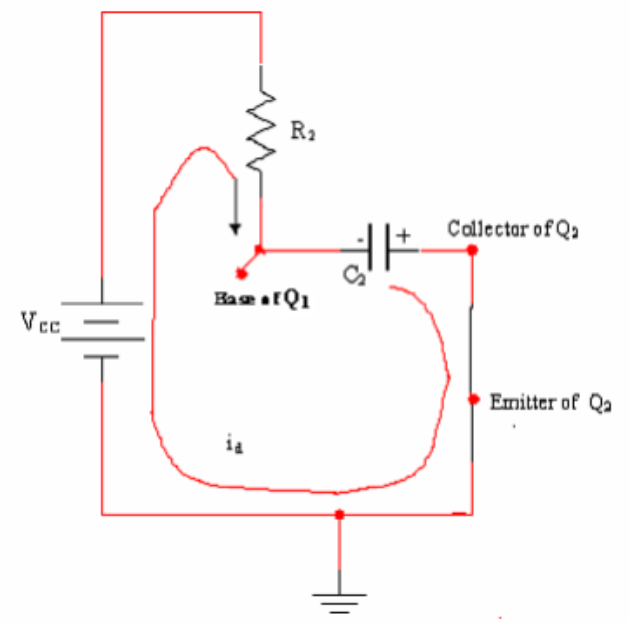
Prior to this condition, Q_2 must have been in the OFF state and Q_1 must have been in the ON state. As a result C_2 must have been charged through R_{C2} . Between the base and emitter terminals of Q_1,



Charging of capacitor C_2

When Q_2 suddenly changes from the OFF state to ON state, the voltage between its collector and emitter terminals is $V_{CE}(\approx 0V)$. Hence the collector of Q_2 is at ground potential i.e. the positive end of the capacitor C_2 is at the ground potential and its negative terminal is connected to base of Q_1. As a large negative voltage is now coupled to base of Q_1, Q_1 is indeed in the OFF state.

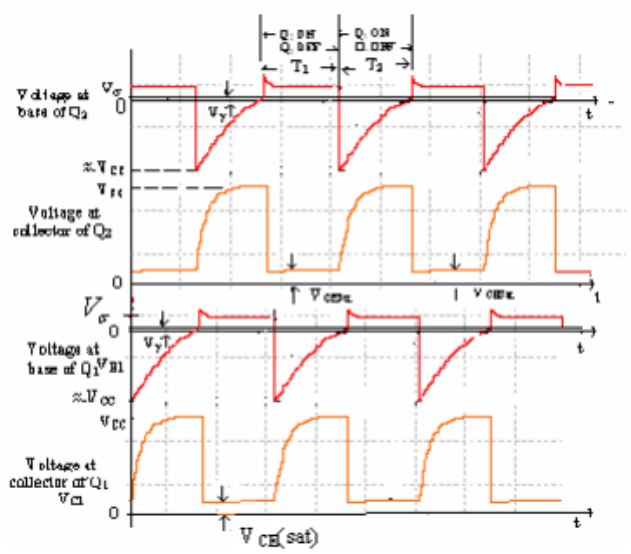
But Q_1 is not going to remain in the OFF state forever. Now, with Q_2 ON, the charge on the capacitor C_2 discharges with a time constant $\tau_2 = R_2C_2$.



discharge of C_2 through R_2

As a result, the voltage at the base of Q_1 goes on changing as a function of time. Once this voltage is V_γ, Q_1 draws base current. Hence there is a collector current; there is a voltage drop across R_{C1} and the voltage at the collector of Q_1 falls. Earlier this voltage was V_{CC} and now it is smaller than V_{CC}. Therefore, the negative step at this collector is coupled to the base of Q_2 through C_1. As the collector of Q_1 and the base of Q_2 are connected through C_1 and as a capacitor will not allow any sudden changes in voltage, whatever is the change that has taken place at the first collector an identical change takes place at the base of Q_2. As a result the base current of Q_2 is reduced, its collector current is reduced and the voltage at its collector rises. This positive step change is coupled to the base of Q_1. Its base current further increases. The collector current increases, the voltage at the collector of Q_1 further falls and this change is coupled to the base Q_2 and this process is repeated. Thus a regenerative action takes place and Q_2 switches into the OFF state and Q_1 goes into the ON state.

The waveforms at the base and collectors of Q_1 and Q_2 are shown below.



Waveforms of collector–coupled astable multi

When suddenly the transistor changes from the OFF state to the ON state there could be a small overshoot at this base and at the collector of the other transistor.

Further, it is seen that when a transistor changes from the ON state into OFF state, say Q_1, its collector voltage is required to abruptly rise to V_{CC}. But when Q_1 is OFF and Q_2 is ON, there is a charging current of capacitor C_1. As a result the voltage V_{C1} will not suddenly rise to V_{CC}. Only when this charging current is zero, the collector voltage reaches V_{CC} . Hence, there is rounding off of the rising edge of the pulse.

Voltage Sweep Generators

Introduction:

A linear time-base generator is one that provides an output waveform a portion of which Exhibits a linear variation of voltage or current with time. Earlier, this waveform is used to sweep the electron beam horizontally across the screen. Because of this reason it is called **sweep voltage**.

Quality of a sweep is specified by three errors that define deviation from linearity.

Errors that define deviation from linearity are three types.

i)the slope error or speed error e_s

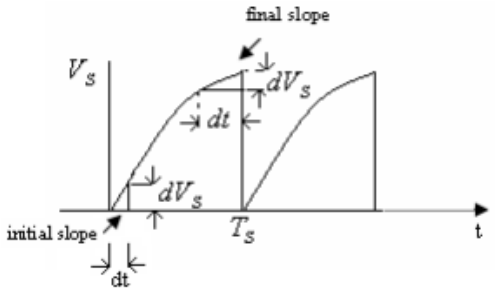
ii)displacement error e_d

iii)tansmission error e_t

(a)Slope or sweep speed error,e_s

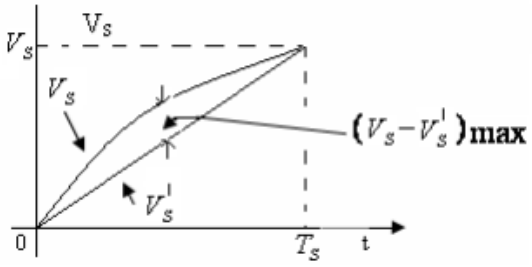
$$e_s = \frac{\text{initial slope} - \text{final slope}}{\text{initial slope}}$$

$$= \frac{\left.\frac{dV_S}{dt}\right|t=0 - \left.\frac{dV_S}{dt}\right|t=T}{\left.\frac{dV_S}{dt}\right|t=0}$$



(b) Displacement error, e_d is the maximum difference between the actual sweep voltage and the linear sweep which posses through the beginning and end points of the a sweep.

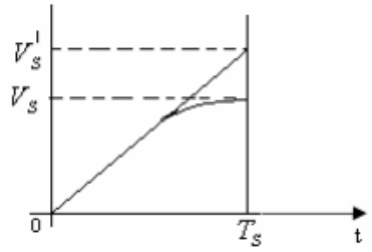
$$e_d = \frac{(V_s - V_s')_{max}}{V_s}$$



(c)Transmission error, e_t

If a ramp voltage is transmitted through a highpass RC circuit, the output falls away from the input.

$$e_t = \frac{(V_s' - V_s)}{V_s'}$$

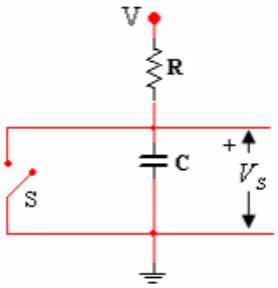


V_s is the actual output

V_s' is the input

(1) Exponential sweep generator: A simple exponential sweep generator and its output are shown in Figs. a) and b) respectively

If initially the capacitor is uncharged and t = 0 the switch S is open, the capacitor charges to the supply voltage V.



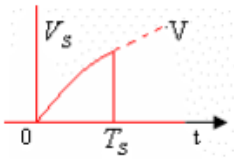
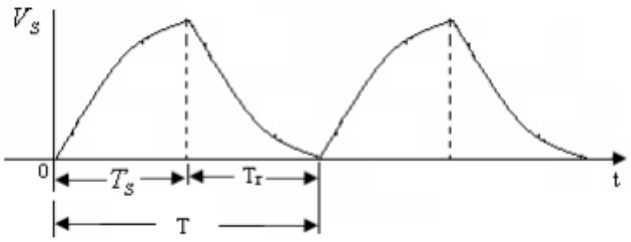


Fig.a) A simple exponential sweep generator Fig.b) Output of the sweep generator

If the resistance offered by the switch is ideally not zero there is a finite time delay before the signal reaches its initial value. This time delay is called flyback time, restoration time or retrace tie.

Normally $T_r << T_s$, so $T \approx T_s$



The voltage variation in the capacitor C is

$$v_c(t) = V_f - (V_f - V_i)e^{-t/\tau}$$
$$= V - (V - 0)e^{-t/\tau}$$
$$v_c(t) = v_s = V(1 - e^{-t/\tau})$$

Assume that after an interval T_s when $v_s = V_s$, the switch closes. The charge on the capacitor discharges with a negligible time constant and the voltage abruptly falls to zero at $t = T_S$.

$$v_s = V(1 - e^{-t/\tau})$$

$$\frac{dv_s}{dt} = -Ve^{-t/\tau}(-\frac{1}{\tau}) = \frac{V}{\tau}e^{-t/\tau}$$

$$\left.\frac{dv_s}{dt}\right|t = 0 \quad = \quad \frac{V}{\tau}$$

$$\left.\frac{dv_s}{dt}\right|t = T_S \quad = \quad \frac{V}{\tau}e^{\frac{-T_S}{\tau}}$$

$$\therefore e_s = \frac{\frac{V}{\tau} - \frac{V}{\tau}e^{\frac{-T_S}{\tau}}}{\frac{V}{\tau}} = \left[1 - e^{\frac{-T_S}{\tau}}\right]$$

at $t = T_S, v_s = V_s$

Hence $$V_s = V\left(1 - e^{\frac{-T_S}{\tau}}\right)$$

$$\therefore 1 - e^{-T_S/\tau} = \frac{V_s}{V}$$

Substituting ,we have

$$e_s = \frac{V_s}{V}$$

From above equation it is evident that e_s is small when V >> V_s. i.e. the linearity improves if V is large when compared to V_s. Therefore, a simple exponential sweep suffers from the disadvantage that a linear sweep is generated only when the sweep amplitude is very much small when compared to the applied d.c. voltage, V

If $\frac{t}{\tau} << 1$

$$e^{-t/\tau} = 1 - \frac{t}{\tau} + \frac{t^2}{2\tau^2} - \frac{t^3}{6\tau^3} + \Lambda$$

$$v_s = V\left(1 - e^{-t/\tau}\right)$$

$$= V\left[1-1+\frac{t}{\tau}-\frac{t^2}{2\tau^2}+\frac{t^3}{6\tau^3}\Lambda\right]$$

$$= \frac{Vt}{\tau}\left[1-\frac{t}{2\tau}+\frac{t^2}{6\tau^2}\right]$$

Since $v_s = V_s$ at $t = T_s$

To first approximation

$$V_s^{'} = \frac{VT_s}{\tau}$$

As this is a linear sweep

$$e_s = \frac{V_s}{V} = \frac{T_s}{\tau}$$

Hence, for e_s to be small $\tau >> T_s$

If the actual sweep is non-linear, consider the first two terms

$$v_s = \frac{Vt}{\tau}\left(1-\frac{t}{2\tau}\right)$$

$$\therefore V_s = \frac{VT_s}{\tau}\left(1-\frac{T_s}{2\tau}\right)$$

This is a non-linear sweep

Therefore the transmission error e_t is

$$e_t = \frac{V_s^{'} - V_s}{V_s^{'}}$$

$$= \frac{\frac{VT_s}{\tau}-\frac{VT_s}{\tau}\left(1-\frac{T_s}{2\tau}\right)}{\frac{VT_s}{\tau}}$$

$$e_t = \frac{T_s}{2\tau}$$

Now,

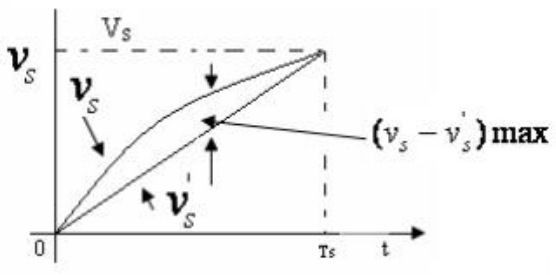
$$e_s = \frac{T_s}{\tau}$$

If we relate e_s and e_t

$$e_t = \frac{T_s}{2\tau} = \frac{e_s}{2}$$

Displacement error, e_d is

$$e_d = \frac{(v_S - v_S')\max}{V_s}$$



From equation 6.12

$$v_s = \frac{Vt}{\tau}\left(1 - \frac{t}{2\tau}\right)$$

$$v_s^1 = \frac{Vt}{\tau}$$

$$(v_s - v_s^1) = \frac{Vt}{\tau} \times \frac{t}{2\tau}$$

The deviation is maximum at $t = \frac{T_s}{2}$

$$(v_s - v_s^1)_{\max} = \frac{VT_s}{2\tau} \times \frac{T_s}{4\tau}$$

$$v_s = \frac{Vt}{\tau}$$

At $t = T_s \quad v_s = V_s$

$$\therefore V_s = \frac{VT_s}{\tau}$$

$$\therefore e_d = \frac{(v_s - v_s^1)_{\max}}{V_s} = \frac{\frac{VT_s}{2\tau} \times \frac{T_s}{4\tau}}{\frac{VT_s}{\tau}}$$

$$= \frac{T_s}{8\tau} = \frac{T_s}{8\tau}$$

$$e_d = \frac{1}{8} e_s$$

The interrelationship between the three types of errors is given below

$$e_d = \frac{1}{8} e_s = \frac{1}{4} e_t$$

If we know one type of error, we can calculate the other types of errors

If the capacitor is charged with a constant current I then the voltage across $C = \frac{I}{C} t$.

Hence, the rate of change of voltage with time is called sweep speed.

Sweep speed = $\frac{I}{C}$

UJT SWEEP

In the exponential sweep generator , a UJT can be used as switch S.
The UJT and its d.c circuit are shown in figs.below. A UJT consists of an N-type semiconductor bar with leads B_1 and B_2 drawn. Emitter is a P-type material and it is heavily doped. Let the bias voltage V_{BB} be applied.

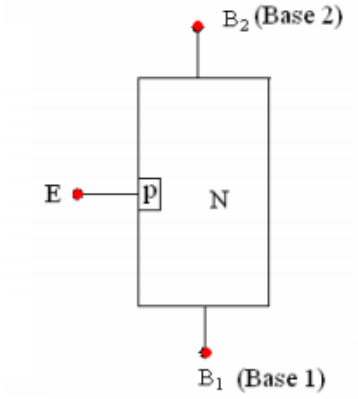


Fig (a) UJT

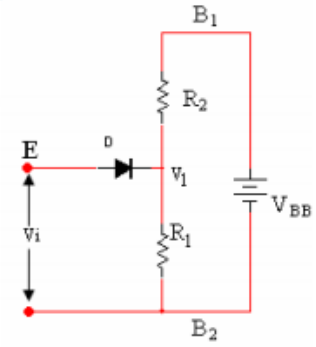


Fig.(b) d.c.circuit

We have, $V_1 = V_{BB}\dfrac{R_1}{R_1 + R_2}$

$= V_{BB}\dfrac{R_1}{R_{BB}} = \eta V_{BB}$

where $\eta =$ Intrinsic stand-of-ratio (lies around 0.7)

As long as $V_i < \eta V_{BB}$, D is OFF.

When $V_1 \geq \eta V_{BB}$ D is ON and a large number of charge carriers exist on the N-side, reducing the resistance and the device conducts heavily, switch S is closed. The V-I characteristic of a UJT is shown in fig.c

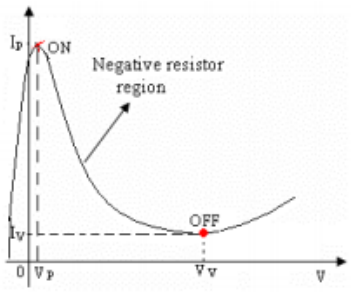


Fig.c. V-I characteristic of UJT

An exponential sweep generator using UJT is shown in fig. c)below,

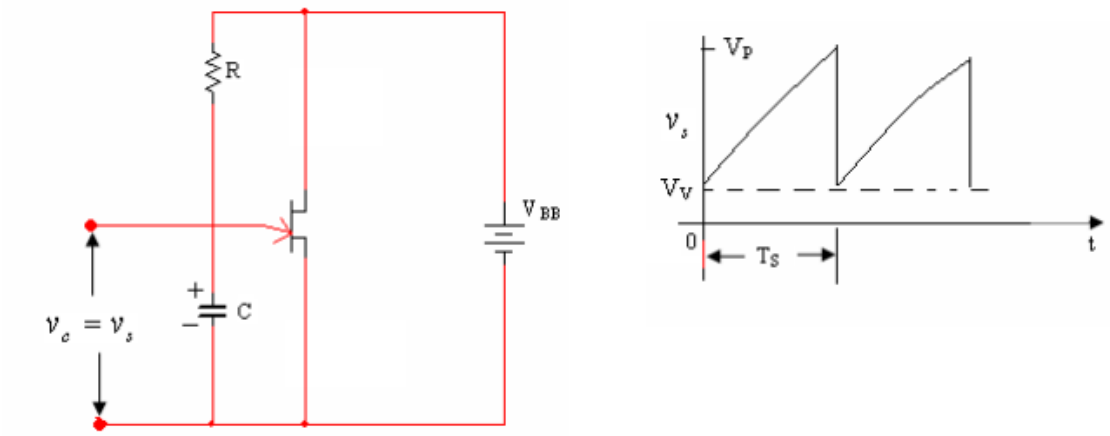


Fig.c A practical UJT sweep generator and its output

$$v_s = V_{BB}\left(1 - e^{-t/\tau}\right)$$

At $t = T_s, v_s = \eta V_{BB}$

$$\eta V_{BB} = V_{BB}\left(1 - e^{-t/\tau}\right)$$

$$V_{BB} e^{-T_s/\tau} = V_{BB}(1-n)$$

$$T_s = \tau \ln \frac{1}{(1-n)}$$

Alternately

$$v_s = V_f - (V_f - V_i)e^{-t/\tau}$$

$$= V_{BB} - (V_{BB} - V_v)e^{-t/\tau}$$

At $t = T_s, v_s = V_s = V_p$

$$V_p = V_{BB} - (V_{BB} - V_v)e^{-T_s/\tau}$$

$$T_s = \tau \ln \frac{(V_{BB} - V_V)}{(V_{BB} - V_P)}$$

TRANSISTOR CONSTANT- CURRENT SWEEP

The sweep voltage generated by an exponential sweep generator is nonlinear as the current in the capacitor varies exponentially. However, to generate a linear sweep, the capacitor is required to charge with a constant current. We have studied the basic transistor configuration CB. The output characteristics of the CB configuration, in fig.a) shows that for a constant value of I_E, Ic is independent of V_{CB} and the curves are parallel to the V_{CB} axis, except for small values of V_{CB}.

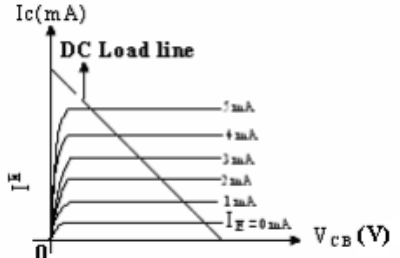


Fig.(a) Output characteristics of CB configuration

It is evident from the above characteristics that if a capacitor is charged using the constant collector current of the CB configuration, the resultant sweep voltage must be a linear sweep voltage. Fig.b shows the circuit of a transistor constant current sweep generator using the CB configuration.

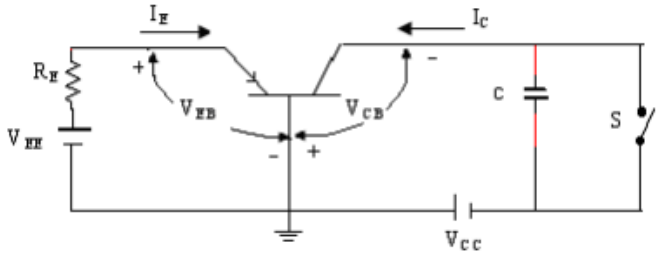


Fig.b CB constant current sweep generator

The current I_E in the base loop is

$$I_E = \frac{V_{EE} - V_{EB}}{R_E}$$

Let the switch S be open at t = 0

The collector current is

$$I_C = h_{FB} I_E \quad \text{and is constant.}$$

Hence C charges with the constant I_C and the voltage across the capacitor varies linearly as a function of time.

To determine the sweep voltage Vs, consider the small signal model of the transistor in CB configuration.fig.c

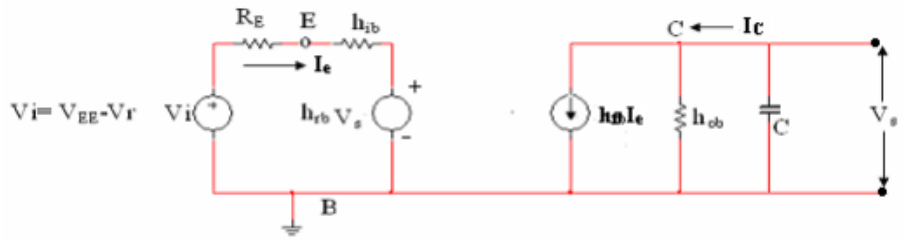


Fig.c Equivalent circuit

Writing the KVL equation of the input loop

$V_i = I_e(R_E + h_{ib}) + h_{rb}V_s = V_i$

Writing the KCL equation at the output node C

$$I_C = h_{fb}I_e + h_{ob}V_S = -C\frac{dV_S}{dt}$$

$$h_{fb}I_e + h_{ob}V_s = -C\frac{dv_s}{dt}$$

$$I_e(R_E + h_{ib}) + h_{rb}V_s = V_i$$

$$\therefore I_e = \frac{V_i - h_{rb}V_s}{R_E + h_{ib}}$$

$$\therefore \frac{-CdV_S}{dt} = h_{fb}\left[\frac{V_i - h_{rb}V_S}{R_E + h_{ib}}\right] + h_{ob}V_s$$

$$\frac{dV_s}{dt} - \frac{h_{fb}}{C}\left[\frac{h_{rb}}{(R_E + h_{ib})}V_S\right] + \frac{h_{fb}V_i}{C(R_E + h_{ib})} + \frac{h_{ob}V_s}{C} = 0$$

$$\frac{dv_s}{dt} + \frac{1}{C}\left[h_{ob} - \frac{h_{fb}h_{rb}}{(R_E + h_{ib})}\right]V_S = \frac{-h_{fb}V_i}{C(R_E + h_{ib})}$$

Let $\alpha = -h_{fb}$ and $\frac{1}{\tau} = \left[h_{ob} + \frac{\alpha h_{rb}}{R_E + h_{ib}}\right]\frac{1}{C}$

$$\therefore \frac{dV_s}{dt} + \frac{1}{\tau}V_s = \frac{\alpha V_i}{C(R_E + h_{ib})}$$

Let $\frac{\alpha V_i}{C(R_E + h_{ib})} = K$

$$\frac{dV_s}{dt} + \frac{1}{\tau}V_s = \mathrm{K}$$

Solving, we have

$V_s(t) = \tau K\left[1 - e^{-t/\tau}\right]$

$$V_s(t) = \frac{\alpha\tau V_i}{C(R_E + h_{ib})}\left(1 - e^{-t/\tau}\right)$$

Expanding $e^{-t/\tau}$ and taking only the first term

$$V_s = \frac{\alpha V_i t}{C(R_E + h_{ib})}$$

But at t = 0, $I_e = \frac{V_i}{R_E + h_{ib}}$

Therefore we have

$$V_s = \frac{\alpha I_e t}{C}$$

At $t = T_s$, $V_s = V_s$

$$\therefore V_S = \frac{\alpha V_i T_s}{(R_E + h_{ib})C}$$

$$\therefore T_s = \frac{CV_s(R_E + h_{ib})}{\alpha V_i}$$

where T_s is the sweep duration and V_s is the sweep amplitude.

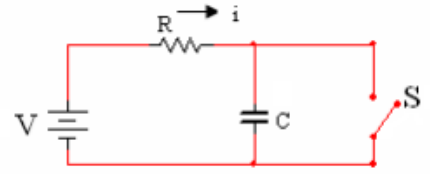
The slope error $e_s = \frac{T_s}{\tau} = \left\{\frac{CV_s(R_E + h_{ib})}{\alpha V_i}\right\}\left\{\frac{1}{C}\left(h_{ib} + \frac{\alpha h_{rb}}{R_E + h_{ib}}\right)\right\}$

$$= \frac{V_s(R_E + h_{ib})h_{ob}}{\alpha V_i} + \frac{h_{rb}V_s}{V_i}$$

$$\therefore e_s = \frac{V_S}{V_i}\left\{h_{rb} + \frac{h_{ob}}{\alpha}(R_E + h_{ib})\right\}$$

TIME-BASE GENERATORS-GENERAL CONSIDERATIONS:

A simple exponential sweep generator essentially produces a nonlinear sweep voltage. Consider an auxiliary generator v. If V always kept equal to the volt across C(i.e. $v = v_C$) Then net voltage in the loop is V. Then $i = \frac{V}{R}$,i.e. the capacitor charging current is constant and perfect linearity is achieved. Let us identify three nodes X, Y and Z. In a circuit one terminal is chosen as a reference terminal or ground terminal. Ground in a circuit is an arbitrarily chosen reference terminal.



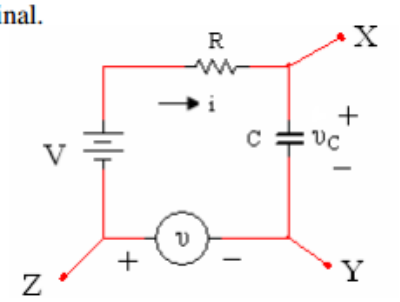


Fig. Method to linearize a non-linear sweep

Miller Sweep:

Now let Z be the ground terminal, and redrawing the above circuit

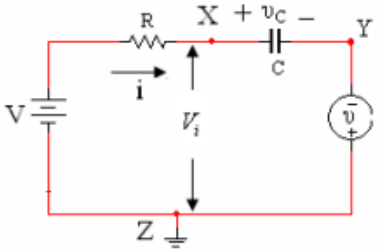
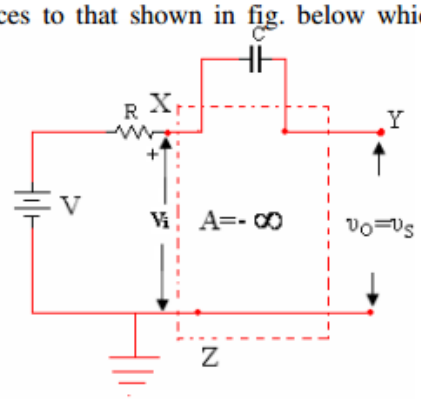


Fig. The sweep generator with Z as the ground terminal

Since $v_c = v$, $V_i = 0$.Hence if the auxiliary generator is replaced by an amplifier with X and Z as input terminals and Y and Z as output terminals, then the gain of the amplifier A should be infinity. The above circuit reduces to that shown in fig. below which is called Miller Sweep .



Bootstrap Sweep: Let Y be the ground terminal redrawing the above circuit and replacing the auxiliary generator by an amplifier with X and Y as input terminals the amplifier should have again of unity as $v = v_C$

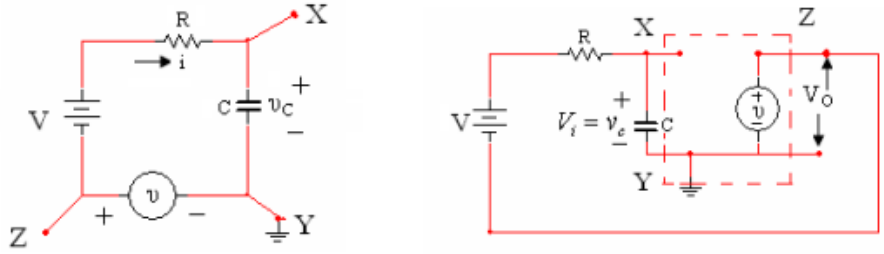


Fig. the sweep generator, with Y as the ground terminal

Replacing the generator by amplifier, the circuit is redrawn as in fig. below

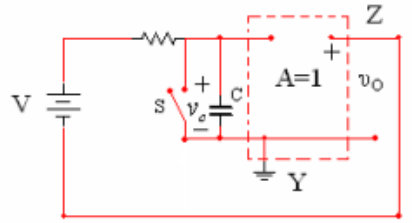
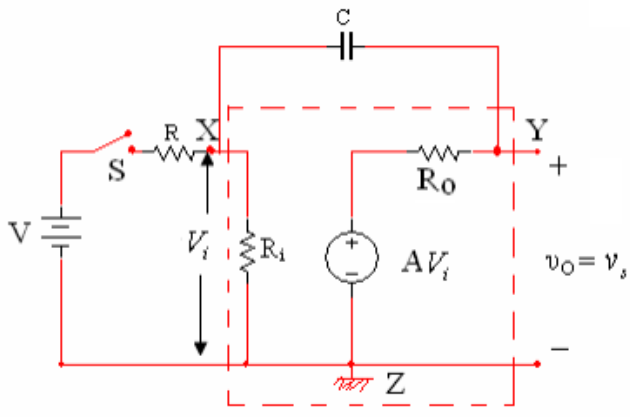


Fig. Bootstrap sweep generator

This type of sweep generator is called a Bootstrap sweep generator

Slope error of a Miller's sweep:

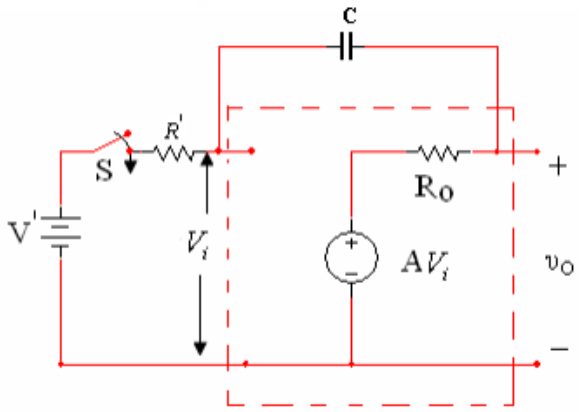


R_i = Input resistance of the amplifier
R_o = Output resistance of the amplifier

Thevenising the circuit at the input

$$V' = V\frac{R_i}{R+R_i} = V\frac{1}{1+\frac{R}{R_i}}$$

$$R' = \frac{R \times R_i}{R+R_i}$$



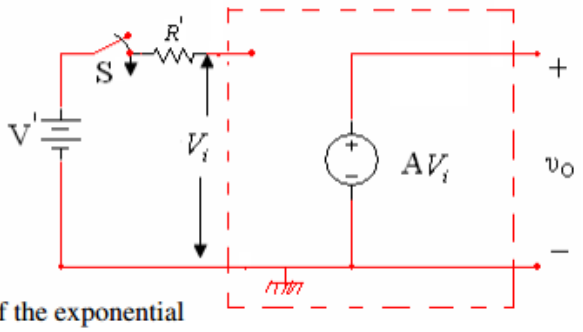
Let $R_o = 0$

At t = 0 the voltage across the capacitor is zero

$\therefore v_i - Av_i = 0, \quad v_i(1-A) = 0, \quad v_i = 0$

$v_i = AV_i = V_o = 0$

As $t \to \infty$, the capacitor is fully charged no current flows in it and hence can be replaced by an open circuit for the purpose of finding out the output voltage. The resultant circuit is



At $t = \infty$, $V_i = V'$

Hence $V_0 = AV'$

We know that $e_s = \frac{V_s}{V}$

where V_s = sweep amplitude

V = total peak to peak excursion of the exponential

Hence, $e_{s_{Miller}} = \frac{V_s}{V_0} = \frac{V_s}{/A/V'} = \frac{V_s}{/A/} \times \frac{1}{V'}$

Substituting , $e_{S_{Miller}} = \frac{V_s}{/A/} \times \frac{1+R/R_i}{V}$

$= \frac{V_s}{V} \times \frac{1+R/R_i}{/A/}$,where $\frac{V_s}{V}$ is the slope error of the exponential sweep.

$\therefore\ e_{s_{Miller}} = e_S \times \frac{1+R/R_i}{|A|}$ .Even if R_i is small, as A is large, the slope error of a Miller's sweep is very small. Hence, for all practical purposes this sweep generator produces a near linear sweep.

Slope error of Bootstrap sweep generator:

Consider the Bootstrap sweep generator in fig I)

If initially the capacitor is uncharged and if S is closed at t = 0

$V_o = -V \times \frac{R_o}{R + R_o}$ from fig.ii)

And as R_o of emitter follower is very small.

$V_0 \approx 0$

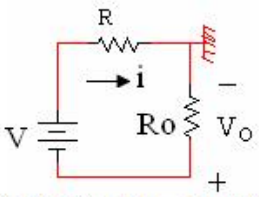


Fig ii) Circuit to calculate the output at t = 0

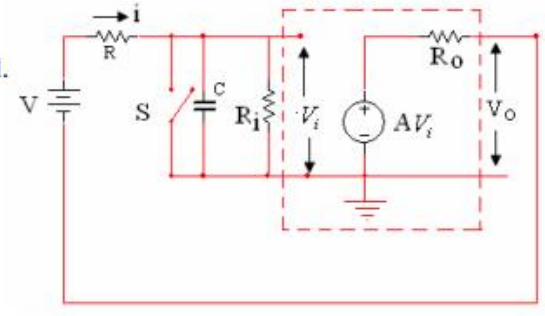


Fig.i) Bootstrap sweepgenerator

As t $\longrightarrow \infty$, C is fully charged and is open circuited, fig.6.20

$$V_0(t \to \infty) = \frac{V(AR_i - R_0)}{R_0 + R + R_i(1 - A)}$$

Dividing by R_i

$$V_0(t \to \infty) = \frac{V(A - R_0/R_i)}{(1 - A) + \frac{R}{R_i} + \frac{R_0}{R_i}}$$

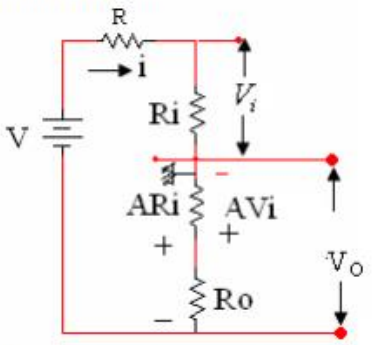


Fig 6.20 circuit to calculate the output as $t \to \infty$

$$V_0(t \to \infty) \approx \frac{V}{(1 - A) + R/R_i}$$

R_o is the output resistance which is small and R_i is its input resistance which is large.

$\therefore \quad \frac{R_0}{R_i}$ is negligible and A ≈ 1

Equation reduces to

$$\therefore e_{sBootstrap} = \frac{V_s}{V}(1 - A + R/R_i)$$

$$\equiv e_S \frac{R}{R_i}$$

If $R=R_i$, $e_{sBootstrap} = e_S$ .That is the Bootstrap circuit will not provide any improvement in linearity. For this sweep to be linear Ri >>R

Transistor Miller Sweep: Consider the working of the triggered transistor Miller's sweep generator as shown below.

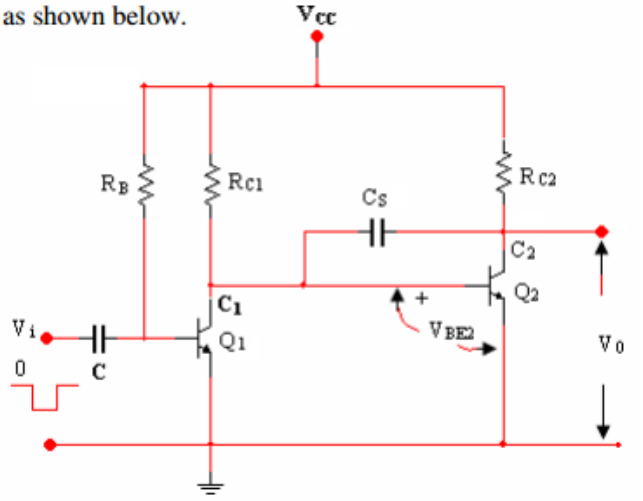


Fig. Transistor Miller sweep

The circuit conditions are adjusted such that when the input is zero Q_1 is ON and is in saturation. Therefore the voltage at C_1 (collector of Q_1) is $V_{CE}(sat) \approx 0$. Transistor Q_2 is OFF since $V_{BE2} \approx 0$. The voltage at C_2 (collector of Q_2) is V_{CC}.

The voltage across the capacitor C_s is V_{CC}. When the input signal goes negative, Q_1 is OFF and the voltage at C_1 rises and Q_2 goes ON. The charge on the capacitor C_s discharges. Hence the output is a negative going ramp. Again at the end of the input pulse, Q_1 goes ON, Q_2 goes OFF and the output again reaches V_{CC}. The waveforms are shown in fig

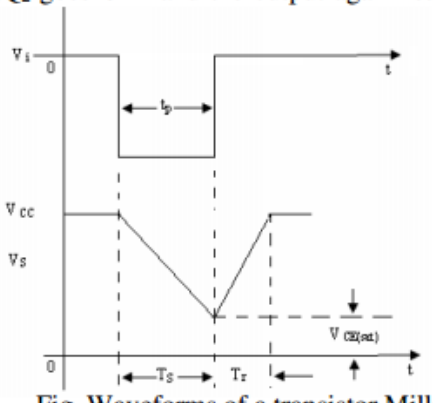


Fig Waveforms of a transistor Miller sweep

Bootstrap circuit: The circuit of a Bootstrap sweep generator is shown in fig.below.

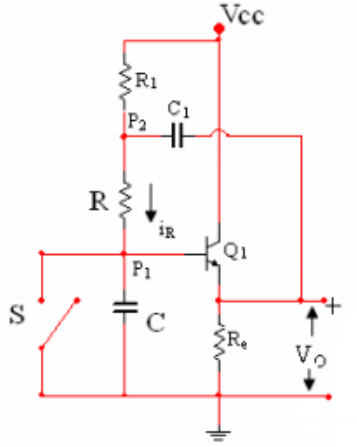


Fig. Bootstrap sweep generator

At t = 0, the switch S is open and the capacitor charges. C_1 is very large. Therefore, it is assumed that the voltage across C_1 remains unaltered during the sweep period. Let the voltage gain of the emitter follower remain constant. Then the voltage at P_2 (output of the emitter follower) follows P_1 (input of the emitter follower). The voltage between P_2 and P_1 will remain invariant and the current i_R through R is constant .As the capacitor charges with a constant current, the resultant sweep is linear.

The circuit of a practical Bootstrap ramp generator is shown.

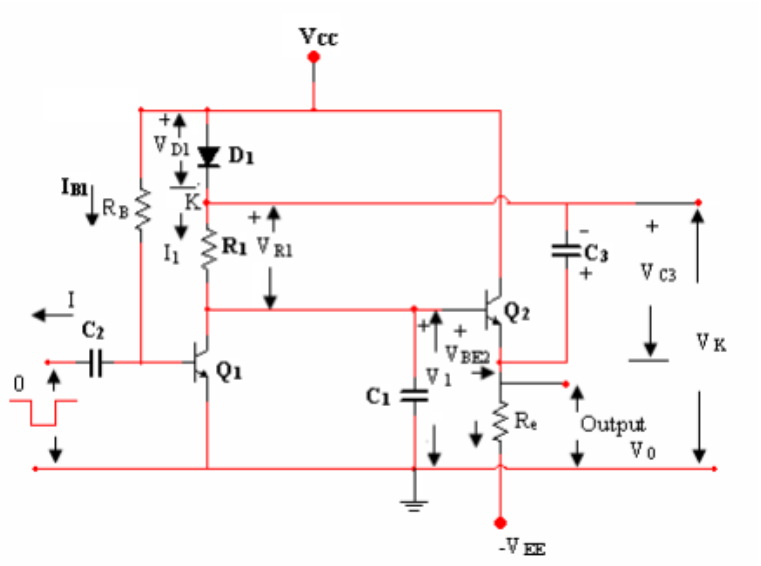


Fig. A practical Bootstrap sweep generator

The ramp is generated across capacitor C_1 which is charged from the current through R_1. The discharge transistor Q_1 when ON keeps the V_1 at $V_{CE}(sat)$ until a negative input pulse is applied. Q_2 is an emitter follower with low output resistance. Emitter resistance R_e is connected to a negative supply V_{EE} instead of referencing to ground to ensure that Q_2 remains conducting even when its base voltage V_1 is close to ground. Capacitor C_3, called bootstrapping capacitance, has a much higher capacitance than C_1. C_3 is meant to maintain a constant voltage across R_1 and thus maintain the charging current constant.

the circuit operation:

Quiescent conditions:

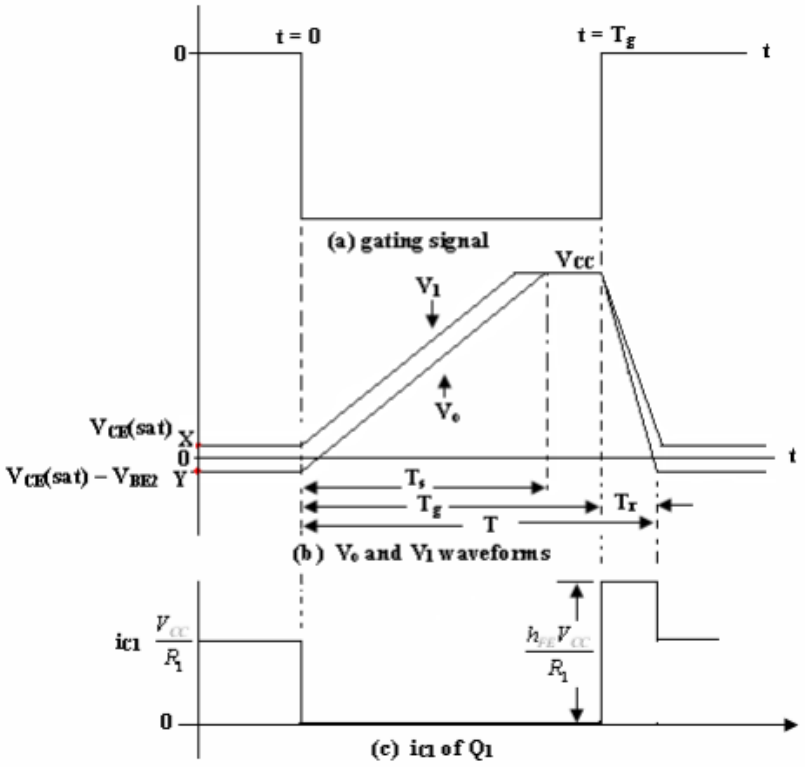


Fig.6.27 waveforms of the bootstrap circuit

As long as the input trigger signal is zero, Q_1 has sufficient base current . So Q_2 goes into saturation. Therefore the voltage V_1 across the capacitor C_1 is $V_{CE}(sat)$.

$$V_1 = V_{CE}(sat)$$

Q_2 is an emitter follower for which input is V_1 and its output V_o is

$V_0 = V_1 - V_{BE2}$

= which is very less

For all practical purposes both V_1 and V_o are zero. The voltage across R_1 is

$$V_{R1} = V_{CC} - V_{D1} - V_{CE}(sat) \approx V_{CC}$$

Also, the voltage across C_3 is $V_{C3} \approx V_{CC}$.

Hence the current I_1 in R_1 is $I_1 = \frac{V_{CC}}{R_1}$

As the base current of Q_2 is smaller than the collector current of Q_1

$$i_{C1} \approx I_1 = \frac{V_{CC}}{R_1} \quad \text{and} \quad I_{B1} = \frac{V_{CC}}{R_B}$$

For Q_1 to be in saturation, $i_{B1(sat)} > i_{B1(active)}$

$$\therefore \frac{V_{CC}}{R_B} > \frac{V_{CC}}{h_{FE} R_1}, \qquad \text{or } R_B < h_{FE} R_1$$

Sweep generation:

At t=0, when voltage at the base of Q_1 goes negative, Q_1 is OFF. There is no current into the collector lead of Q_1 and instead this current flows through C_1 charging it. As the voltage across the capacitor C_1 varies as $\frac{i}{C} t$ and so does the output.

$$V_0 = \frac{V_{CC}}{R_1} \cdot \frac{t}{C_1}$$

When the sweep starts, D_1 is reverse biased and is an open circuit. The changing current I_1 to C_1 through R_1 is supplied by C_3 which is charged to V_{CC}

It is known that the output V_0 varies linearly only when the duration of the gate signal (T_g) is small so that in this period V_0 does not reach V_{CC}. However , if T_g is large, the output V_0 may reach V_{CC} even before T_g. When $V_0 = V_{CC}$, the voltage V_{CE2} of Q_2 is practically zero (saturation). Q_2 no longer behaves as an emitter follower. V_0 and V_1 therefore remain at V_{CC}. The current $\frac{V_{CC}}{R_1}$ now flows through C_3, R_1 and through the base emitter diode of Q_2.therby changing voltage across C_3 by a small amount (ΔV).

If $T_s < T_g$ (ie V_0 reaches V_{CC} before T_g)

Then at $t = T_s$, $V_s = V_{CC}$

Hence $V_{CC} = \frac{V_{CC} T_s}{RC}$, or $T_s = RC$

On the otherhand if $V_s < V_{CC}$, the maximum ramp voltage is

$$V_s = \frac{V_{CC} T_g}{RC}$$

Calculation of retrace time, T_r :

At the end of the gate signal at t=T_g, a current $I_{B1} = \frac{V_{CC}}{R_B}$ again flows into the base terminal of Q_1. Q_1 once again tries to go into saturation. But till such time that V_{CE} of Q_1 is $V_{CE}(sat)$ (Q_1 in saturation), the collector current , C_1 remains constant at

$$i_{C1} = h_{FE} \cdot \frac{V_{CC}}{R_B}$$

The current i_{R1} through R_1 and the discharging current i_a of C_1 now constitute i_{C1}, neglecting the small base current of Q_2

$i_{C1} = i_{R1} + i_a$ and

i_{R1} remains approximately at $\frac{V_{CC}}{R_1}$ and the capacitor discharges with a constant current i_a

The voltage across C_1 falls, and consequently V_o falls since once again Q_2 behaves as an emitter follower.

The discharge current i_d from above equation is

$i_a = i_{C1} - i_{R1}$

$$i_a = \frac{h_{FE} V_{CC}}{R_B} - \frac{V_{CC}}{R_1}$$

Therefore V_1 and V_0 fall linearly to the initial value.The voltage variation during the retrace time T_r is

$V_S = \frac{i_d T_r}{C_1}$, therefore $\therefore T_r = \frac{C_1 V_s}{i_d}$

$$T_r = \frac{C_1 V_s}{V_{CC}\left(\frac{h_{FE}}{R_B} - \frac{1}{R_1}\right)} = \frac{C_1 \frac{V_S}{V_{CC}}}{\left(\frac{h_{FE}}{R_B} - \frac{1}{R_1}\right)}$$

.

Current Sweep Generators

Introduction:

Application of electromagnetic deflection is used in these current sweep generators. When a voltage is applied to a coil of inductance L, the current in L increases linearly with time. Usually a coil or set of coils called yoke is mounted external to the gun structure of the tube and the current in yoke produces a magnetic field that causes deflection of the electron beam.

If at a time t = 0, a voltage V is applied to a coil of inductance L in which the current is initially zero, then the inductor current i_L will increase linearly with time according to $i_L = \frac{V}{L}t$ (In a capacitor $V = \frac{I}{C}t$). A time base circuit using this principle is shown in fig.a

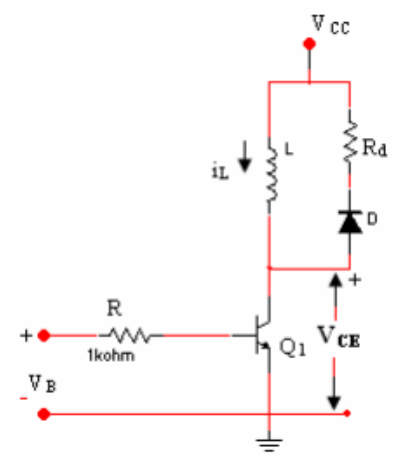


Fig.a Current sweep generator

Fig.b waveforms of a current sweep

The gating waveform V_B operates between two levels. The lower level keeps the transistor in cut off while the upper level drives the transistor into saturation.

As long as the input is negative Q_1 is biased OFF and the inductor current is zero. At t=0+ as the input goes positive Q_1 is driven into saturation. The current i_L increases linearly with time. During the sweep period the diode D does not conduct since it is reverse-biased. The sweep terminates at $t = T_S$ when the trigger signal drives the transistor to cut off. The inductor current then continues to flow through the diode D and the resistance R_d till it decays to zero. This decay is exponential with a time constant $\tau = \frac{L}{R_d}$ where R_d is the sum of the damping resistance and the diode forward resistance.

The inductor current attains a maximum value of I_L in fig b.

Before the transistor is turned ON, and sometime after it has been turned OFF, $V_{CE} = V_{CC}$. When the transistor is ON, $V_{CE} = V_{CE}(sat)$, very low. At t=T_s Q_1 is turned OFF.A spike of amplitude $I_L R_d$ appears across the inductance L. This peak voltage must be limited to make sure that it would not exceed the break down voltage of the collector base junction. I_L is normally chosen on deflection requirements, and a spike of magnitude $I_L R_d$ is generated. Thus there is an upper limit to the size of R_d. The spike decays with

the same time constant as the inductor current. Thus we see that the spike duration depends on L, whereas the spike amplitude does not.

So far we have neglected the resistance of the inductor R_L and the collector saturation resistance of the transistor, R_{CS}.

Taking R_L and R_{CS} into account

$$i_L = \frac{V_{CC}}{R_L + R_{CS}}(1 - e^{\frac{-(R_L+R_{CS})t}{L}})$$

Expanding it in to series

$$i_L \approx \frac{V_{CC}}{R_L + R_{CS}}\left[1 - 1\frac{+(R_L + R_{CS})t}{L} - \frac{(R_L + R_{CS})^2 t^2}{2L^2}\right]$$

$$i_L = \frac{V_{CC}}{L} t\left[1 - \frac{1}{2}\frac{(R_L + R_{CS})t}{L}\right]$$

The slope error e_s is $e_s = \dfrac{I_L}{V_{CC}/(R_L + R_{CS})} = \dfrac{(R_L + R_{CS})I_L}{V_{CC}}$

The current sweep is linear if the slope error is small. Therefore, to ensure linearity the voltage $(R_L + R_{CS})I_L$ must be small when compared with the supply voltage V_{CC}.

As this simple current sweep may not produce a linear output, we may think of methods that help in linearising the sweep. One simple method to produce a linear current sweep is by adjusting the driving waveform.

Linearity correction through adjustment of the driving waveform:

The non-linearity encountered in this circuit results from the fact that as the yoke current increases the current in the series resistance also increases. Consequently the voltage across the yoke decreases and the rate of changeof current decreases. We may compensate for the voltage developed across the resistance as shown in fig.c

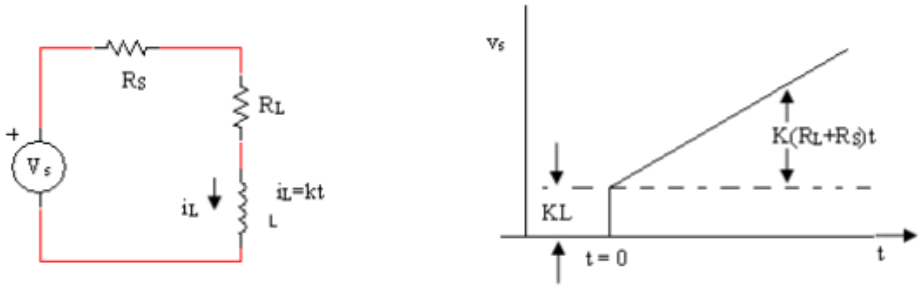


Fig.c Driving waveform for generating a linear current sweep

Let R_s be the internal resistance of the source V_s. The total circuit resistance $(R_S + R_L)$.we want the inductor current to vary linearly

i.e. $i_L = Kt$, where K is the constant of proportionality.

If $i_L = Kt$,then the source voltage V_S is

$$V_S = L\frac{di_L}{dt} + (R_s + R_L)i_L$$

If $i_L = Kt$, $\frac{di_L}{dt} = K$

$$\therefore V_S = LK + (R_s + R_L)Kt$$

This waveform consists of a step by followed by a ramp $(R_s + R_L)Kt$. Such a waveform is called a trapezoidal waveform.

The Norton representation of the driving source, using above equation

$$i_S = \frac{V_S}{R_S} = \frac{LK}{R_S} + (1 + \frac{R_L}{R_S})Kt$$

The waveform of this current source is also a step followed by a ramp, as shown in fig d.

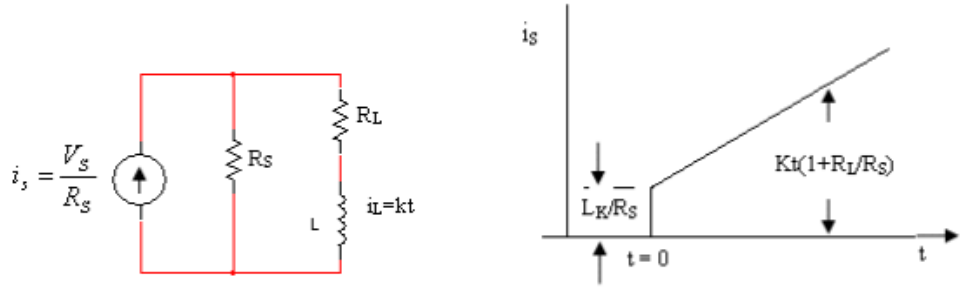


Fig.d Trapezoidal current source and the wave form

Thus a trapezoidal driving waveform generates a linear current sweep. At the end of the sweep the current once again will return to zero exponentially with a time constant

$$\tau = \frac{L}{R_S + R_L}.$$

Generally, $R_S >> R_L$ hence $\tau \approx \frac{L}{R_S}$

If R_S is small the current will decay slowly and a long period will have to elapse before another sweep is possible. But the advantage is that, the peak voltage developed across the current source (transistor) will be small.

Alternately, if R_S is large, the current will decay rapidly, but a large peak voltage will appear across the source.

Generally, one has to strike a compromise such that the spike amplitude is not appreciably large and at the time the inductor current decays in a smaller time interval. To achieve this normally a damping resistance R_d is connected across the yoke to limit the peak voltage.

Let R be the parallel combination of R_S and R_d. Then the retrace time constant is $\tau_r = L/R$.

Now, how to generate this trapezoidal waveform which when applied as a driving source will result in the linearity of the current sweep.

The trapezoidal waveform required is generated using the circuit in fig e.

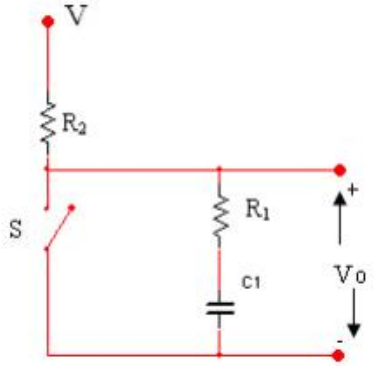


Fig e Generation of trapezoidal waveform

$$v_o = V - \frac{R_2}{R_1 + R_2} V e^{-t/(R_1+R_2)C_1}$$

Generally

$R_2 >> R_1$

$$v_o = \frac{V(R_1 + R_2) - R_2 V e^{-t/(R_1+R_2)C_1}}{R_1 + R_2}$$

Dividing by R_2

$$v_o = \frac{V(1+\frac{R_1}{R_2}) - Ve^{-t/(R_1+R_2)C_1}}{R_1/R_2+1}$$

$$\approx \frac{VR_1}{R_2} + V - Ve^{-t/R_2C_1}$$

$$= \frac{VR_1}{R_2} + V(1 - Ve^{-t/R_2C_1})$$

$$v_0 = V\frac{R_1}{R_2} + \frac{Vt}{R_2C_1}(1 - \frac{t}{2R_2C_1})$$

If $\frac{t}{2R_2C_1} << 1$

$$v_0 = V\frac{R_1}{R_2} + \frac{Vt}{R_2C_1}$$

Thus v_0 is a step followed by ramp.

PRACTICAL LINEAR CURRENT SWEEP GENERATOR

A practical linear transistor current sweep is shown in fig below.

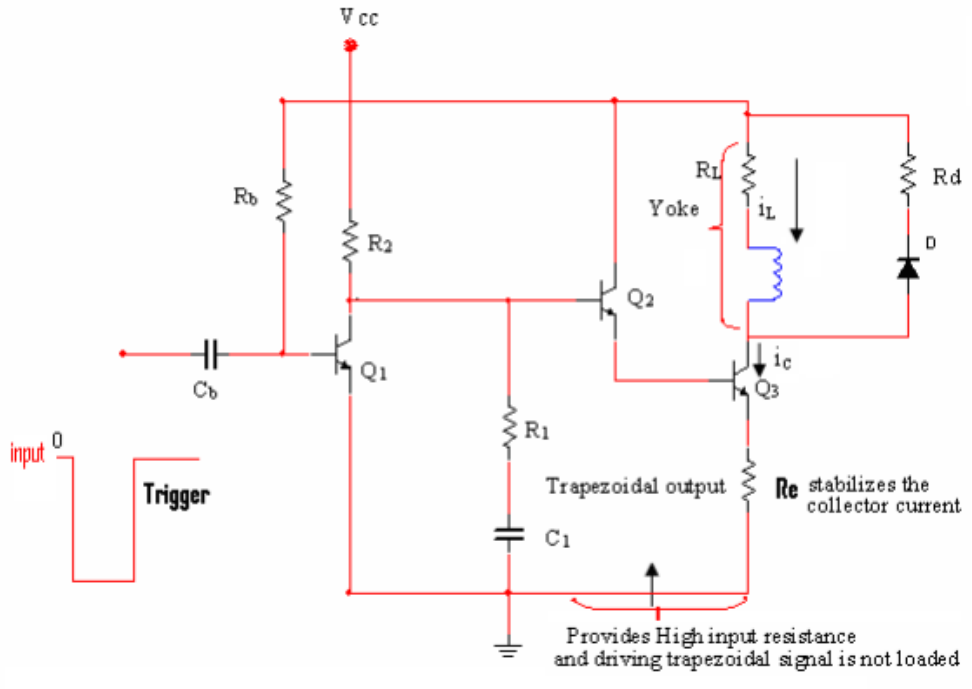


Fig. A practical linear current sweep generator

Q_1 acts as switch-It is ON when the input zero and is OFF when the input goes negative.R_1,R_2 and C_1 generate the trapezoidal driving waveform .Q_2 and Q_3 combination is a Darlington pair and R_E stabilizes i_L. The emitter follower provides large input resistance thus eliminating loading on the driving source by its input. The current i_L varies linearly with time.

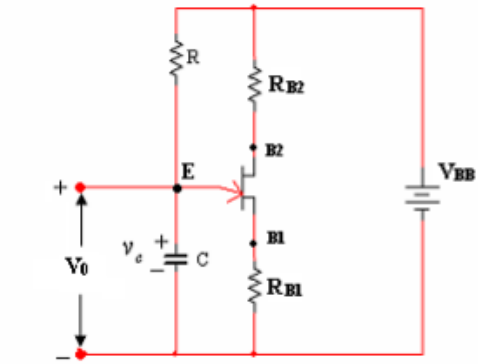
SYNCHRONIZATION AND FREQUENCY DIVISION

In a pulse or a digital system, the waveform generators should run in synchronism or in step with one another i.e. they arrive at some reference point in their cycle at the same time. The waveforms arrive at some reference point in their cycles at the same time. Then these generators are said to be running in synchronism. One generator may complete only one cycle whereas the other generators may complete exactly some integral number of cycles.

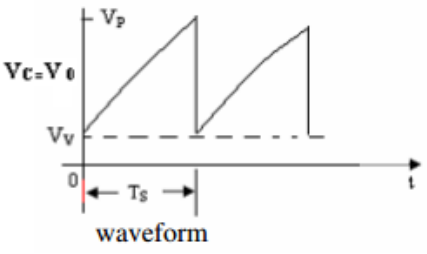
Pulse synchronization of relaxation devices:

Consider a circuit where a capacitor C charges during a finite time interval and is terminated abruptly by the discharge of the capacitor. Such a circuit is called a relaxation circuit.

Consider a UJT relaxation oscillator shown in fig.

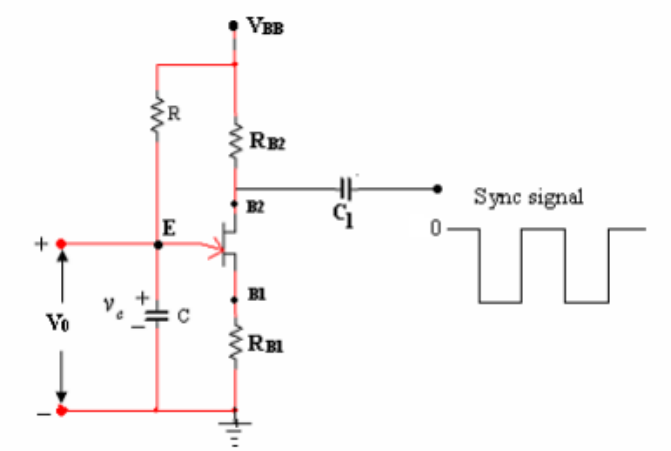


UJT relaxation oscillator



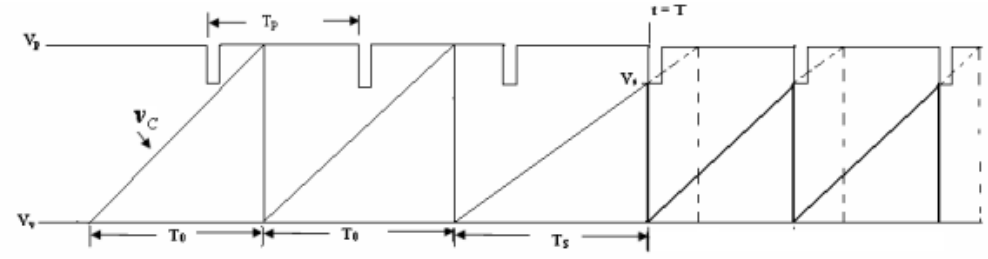
waveform

Here the UJT switch is open so that the capacitor tries to charge to V_{BB}. The moment the voltage across C reaches V_P, the switch closes, allowing the charge on the capacitor C to discharge almost completely. Again, when the voltage across C reaches V_V , the switch opens, again the capacitor charges. This process is repeated, resulting in a waveform as shown in fig.above. To synchronize this device with an external signal, the external signal called the sync signal is connected such that this changes the peak voltageV_P. Thus in a UJT, the sync signal (negative pulse) is applied at B_2 to lower V_P.



Synchronisation of a relaxation device with external pulses

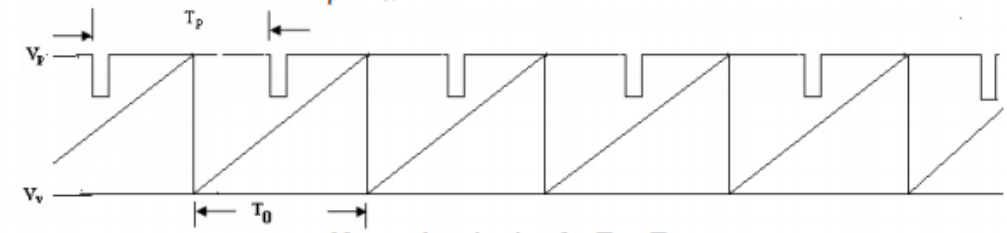
Consider the situation when the synchronizing pulses are applied. Synchronous pulses lowers the peak or breakdown voltage for the duration of the pulse. A regularly spaced pulse train, having a certain amplitude is shown, starting at t = 0.For the first few cycles of the sweep generator output, no synchronization is seen to be effected and the sweep generator runs at a frequency $f_o(=1/T_o)$. At time t = T, the negative pulse reduces the peak and the relaxation device goes ON. From now onwards the sweep generator output and the pulse train run in synchronism.



Synchronization takes place after a few cycles

Thus it observed that the unsynchronized generators run in synchronism after a few cycles. Synchronization takes place only when the sync pulse occurs at a time when it would terminate the sweep cycle prematurely. This means that for synchronization to occur, the interval between the pulses, T_p must be less than the sweep duration T_0.

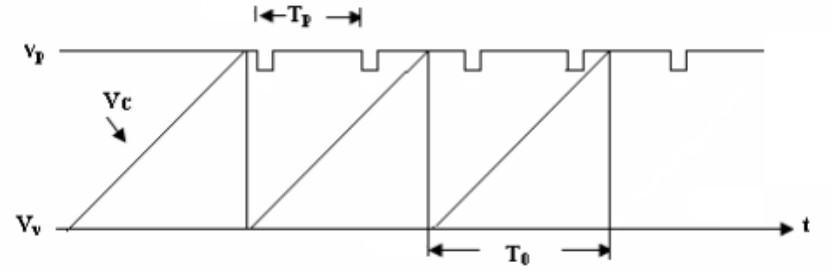
Now consider a case where $T_p > T_0$, .



No synchronization for $T_p > T_0$

Here, $T_p > T_0$ and sync pulses occur at such instants that they will not be able to prematurely terminate the sweep cycle. Hence no synchronization is possible between these two waveform generators. Obviously, synchronization cannot take place as T_p is greater than T_0.

Consider another situation where $T_p < T_0$, but the amplitude of the sync pulses is small as shown in fig.

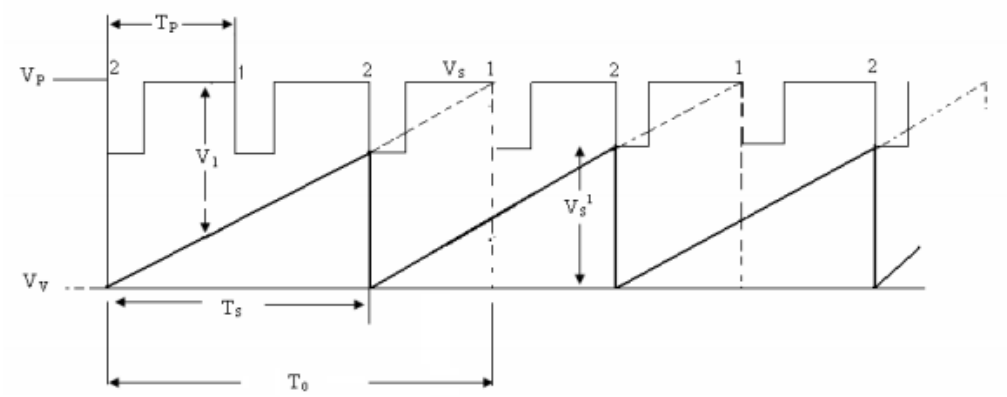


No synchronization is possible if the amplitude of the sync pulses is small

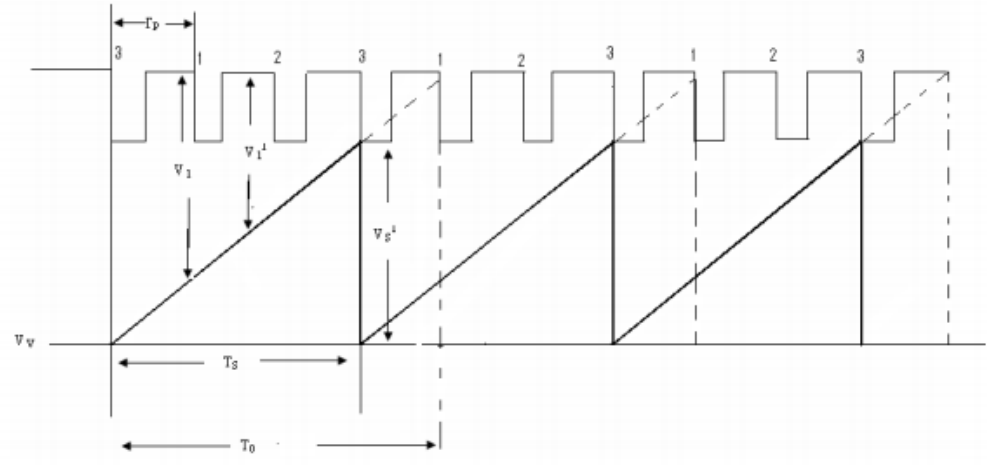
Though, in the present case, $T_p < T_0$, as the amplitude of the sync pulses is small, they will not be able to prematurely terminate the sweep cycle. Hence , no synchronization is possible.

Frequency division in a sweep circuit:

Consider fig.(a) with $T_p < T_0$. The pulse amplitude is not sufficiently large enough to permit each pulse to terminate a cycle. But pulses marked 1 occur at such time intervals that they require large amplitude to terminate a cycle. However, pulses marked '2' have the same amplitude as pulses marked '1'but they occur at such time instants that they are able to prematurely terminate a cycle. The sweep generator is now called a divider, the division factor being 2. This means that there is one sweep cycle for every two sync pulses, i.e. $T_S / T_p = 2$, where T_S is the sweep duration after synchronization and T_p is the spacing between the sync pulses.



(a) Frequency division by 2.



(b) Frequency division by 3 in a sweep generator.

Consider fig.(b) where pulses 1 and 2 are not sufficiently large enough to terminate the cycle. Only when amplitude of the pulse1 is as large as V_1 and that for pulse 2, V_1', they will be able to terminate the cycle prematurely to effect synchronization. However, pulses marked '3' occur at such an instant and have such a magnitude that they will be able to

effect synchronization. Hence for every three sync pulses the sweep generator completes one cycle. Therefore frequency division is said to have occurred by a factor 3.

Synchronization of Astable blocking oscillator: Synchronization of the output of an astable blocking oscillator with frequency division by a factor 4 using positive sync triggers is illustrated in fig. a. The positive sync pulses appear at the collectors of Q_1 and Q_2 as negative pulses, because of polarity inversion in CE configuration. These negative pulses appear as positive pulses at the base of Q_1. A regenerative action takes place, the transistor Q_1 is quickly driven into saturation, and a pulse of duration t_p is generated. During this period of pulse generation, capacitor C_1 charges, the voltage across the capacitor at $t = t_p$ being V_1. Q_1 now goes into the OFF state. As a result the charge on C_1 discharges through R_1 and when the voltage across the capacitor terminals falls to $V_{BB} - V_\gamma$,then Q_1 is again ON and C_1 charges and this process is repeated. The output has a time period T_o, fig. a

But now, in the presence of positive sync pulses at the base Q_1, pulse 4 occurs at such an instant and has such amplitude that it prematurely terminates the cycle when regenerative action again takes place driving the device Q_1 is ON.C_1 again charges and continues. Thus the cycle is prematurely terminated at T_s, and a new cycle repeats. Synchronization with 4:1 division is accomplished.

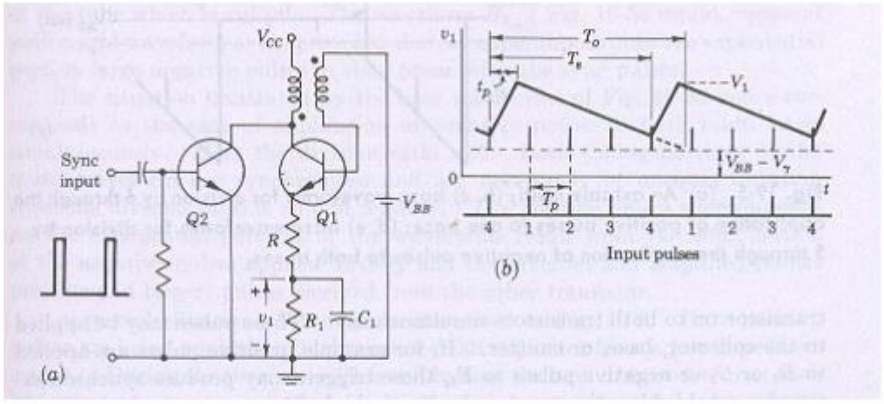
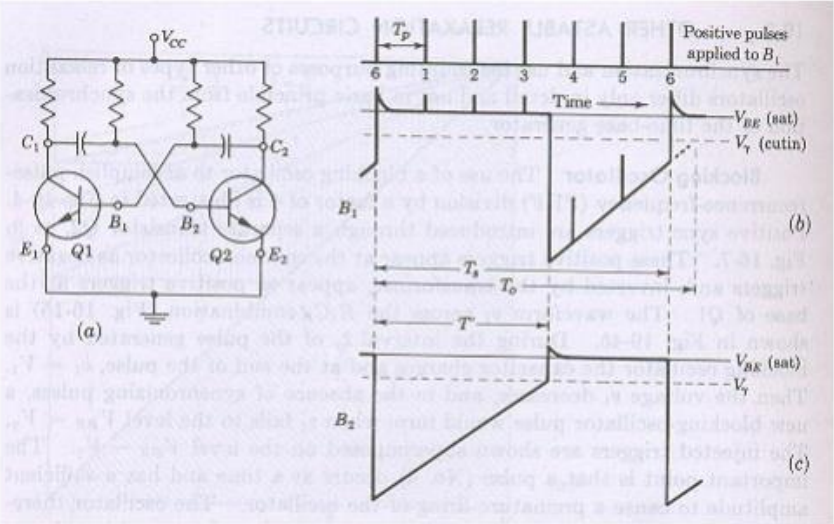


Fig.(b) 4:1 synchronization in an Astable blocking oscillator

Synchronization of a transistor astable multivibrator:

The astable multi in fig.a.may be synchronized or used as a divider by applying positive or negative triggering pulses to both the transistors or to any of the transistor simultaneously.



Fig(b) waveforms

Fig.(b) waveforms to achieve synchronization with frequency divisions of 6:1 positive pulses are applied at the base B_1 of Q_1.to astable multi shown in fig.(b)

In the absence of sync pulses the astable must have had a time period T_0 when the cycle would have naturally terminated at $V_{B1} = V_\gamma$, But the 6th pulse prematurely terminates the natural cycle as this pulse drives the base of Q_1 positive and hence Q_1 goes ON. The new time period is T_S. Here in this arrangement the multivibrator completes one cycle for every six sync pulses. However, though the complete period is synchronized, the individual time periods are not synchronized. T_2 is the same as without synchronization.

Consider Positive pulses applied to B_1 through a small capacitor from a low impedance source. During the period when Q_1 is ON, as the time constant of the pulse input is very small, the pulse is quasi-differentiated. The negative spike is amplified and inverted by Q_1 and this appears as a positive spike during the exponential variation at B_2. The positive spike appearing at the trailing edge of the third input pulse will prematurely terminate the OFF period of Q_2. During the exponential variation of the voltage at B_1 the positive pulses are superimposed and at the leading edge of the sixth pulse, the OFF period of Q_1 is prematurely terminated. Thus not only the entire cycle of the astable is synchronized

with a frequency division of 6:1 but the individual time periods are also synchronized with a division of 3:1.fig.©

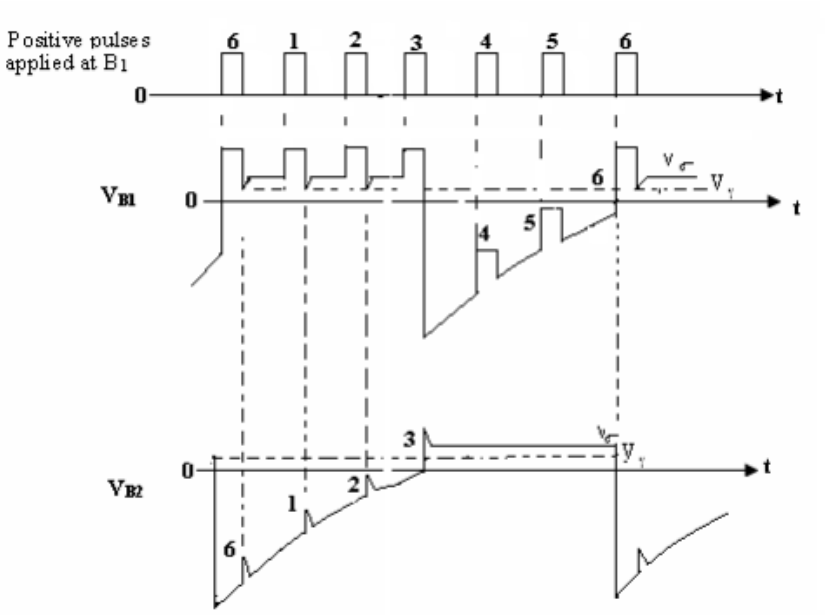


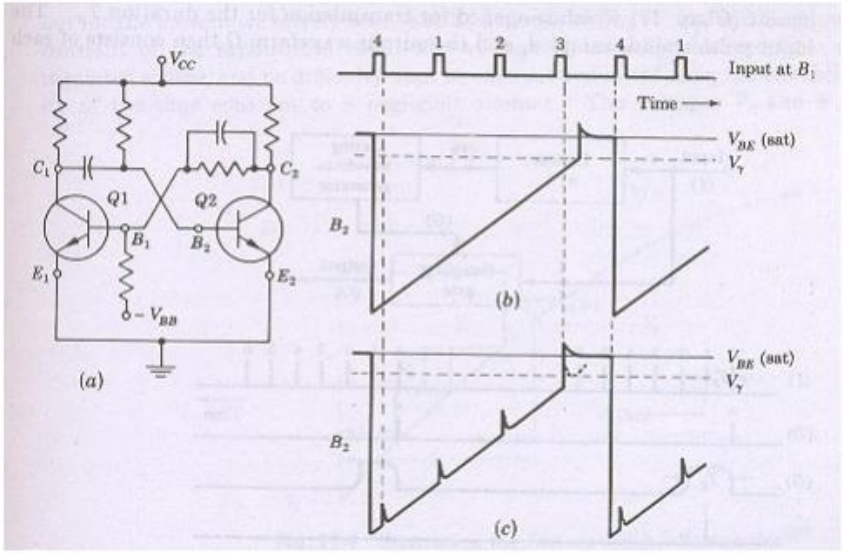
Fig.c. Synchronization of both portions of an astable multi with positive pulses applied at B_1 through a small capacitor and low impedance source.

Monostable relaxation circuit as a divider:

Input pulses may be applied at B1 or C1, depending on the polarity.

If positive pulse train is applied at B_1 through a small capacitance from a low impedance source, a situation may arise similar to astable multi vibrator. Here the overshoot due to differentiation of the input pulse may serve to terminate the timing cycle prematurely as shown in fig C.

In this case two portions of the multi waveform will be synchronized. In this later case the counting ratio will change with increasing amplitude of pulse input. If the overshoot is large enough, the exponential will be terminated by the overshoot at a pulse 2 or pulse 1, in which case the counting ratio will become 3 or 2. Finally, with a large enough overshoot, the timing portion will terminate at the trailing edge of pulse 4 and the circuit will not operate as a multi at all.

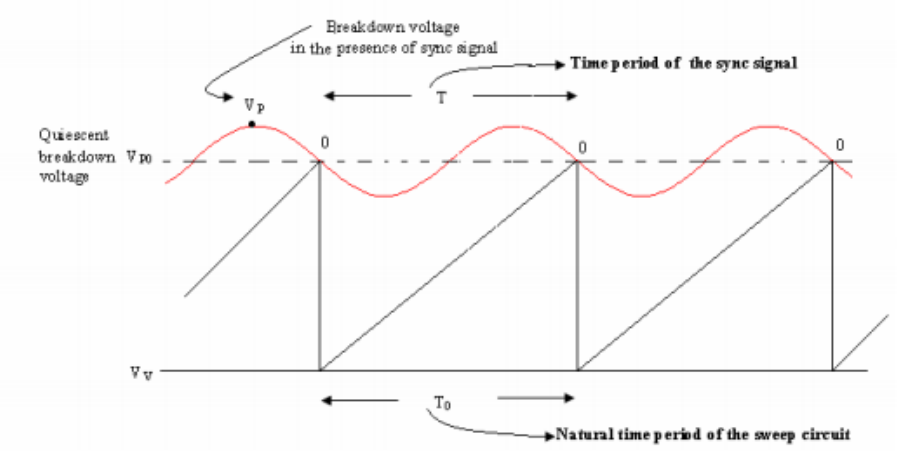


Synchronization of a sweep circuit with symmetrical signals:

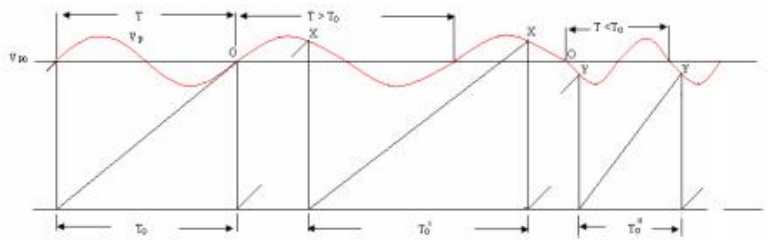
Sinusoidal Sync Signal Consider the sweep generator of Figure which uses a current-controlled negative-resistance device as a switch. assume for simplicity that, as a result of the sync signal, the breakdown voltage of the switch varies sinusoidally. The polarity and precise waveform required of the sync signal for such sinusoidal variation will depend on the particular negative-resistance device being employed. It is to be noted that the circuit behavior to be described does not depend on the sinusoidal a nature of the breakdown-voltage variation. The results depend only on the relatively gradual variation of the breakdown voltage, in contrast to the abrupt variation with pulse-type sync signals

In Fig the dashed voltage level V_{P0} is the breakdown voltage of the negative-resistance device in the absence of a sync signal and the solid curve V_P is the breakdown voltage in the presence of the sync signal. The sync signal has a period T (corresponding to T_p in Fig.), and the natural period is T_o. Consider that synchronization has been established with $T = T_o$. Such synchronization requires that the period of the sweep shall not be changed by the sync signal. Hence, the voltages which mark the limits of the excursion of the sweep voltage must remain unaltered. The sweep cycle must therefore continue to terminate at V_{po}. This means that the intersection of the sweep voltage with the waveform V_p must occur, as shown in Fig at the time when $V\,p$ crosses V_{po}, at the points labeled 0 in the figure. The possibility that the sweep will terminate at the points marked 0' will be considered shortly.)

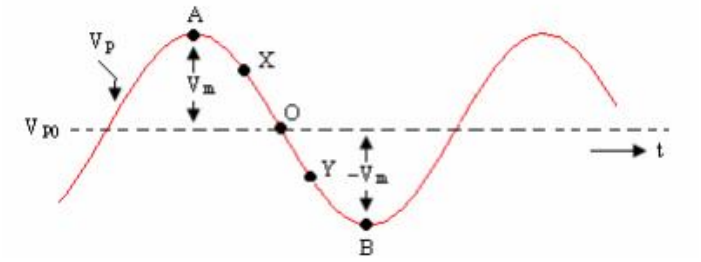
In the case of sync-signal period was equal to or less than the natural period. Actually a pulse could serve reliably only to terminate a timing cycle prematurely and not to lengthen it, In the present case, synchronization is possible both when $T < T_0$ and when $T > T_0$. The timing relationship between the sweep voltage and the breakdown voltage for both cases is shown in Fig. The sweep voltage, drawn as a solid line, has a natural period $T_0' > T$. The sweep voltage meets the V_P curve at a point below V_{PO} and is consequently prematurely terminated. The dashed sweep voltage has a natural period $T_0'' < T$. this sweep meets the curve at a point above V_{PO} and is consequently lengthened. In each case the synchronized period T_S equals the period T.



Synchronization of sweep generator with sinusoidal sync signal



(a) $T = T_O$ (b) $T_o' > T_O$ (c) $T_o'' < T_O$



synchronization when $T \neq T_O$

Sine-wave Frequency Division with a sweep circuit:

The operation of a sweep circuit as a divider is a natural extension of the "Process of synchronization. Figure 19-13 (solid lines) shows the sweep and synchronizing waveforms for division by a factor of 4. This case is one in which the natural period *To* is slightly smaller than *4T*. The sync signal changes the sweep period from *To* to *T.*, where *T.* = *4T*. The dashed waveforms in Fig. 19-13 show that, for the situation illustrated, an increase in amplitude of the sync signal can change the counting ratio from 4 to3. If the sweep terminates on the descending portion of the V_P curve and if as a consequence the period T_0 is lengthened or shortened to T_S, where $T_S = nT$, then the circuit will operate stably as an n:1 counter.

it was tacitly assumed earlier that the range of synchronization extends from the point where the sweep intersects the V_P curve. Such a result normally holds for small values fo sync voltage, but not when the sync amplitude is comparable to the sweep amplitude. In fig. that the sweep will never be able to terminate at a maximum of V_P since to do so would reqired that the sweep first cross the previous negative excursion of the V_P waveform. figure illustrates a case (dashed sweep) where the sync amplitude is in

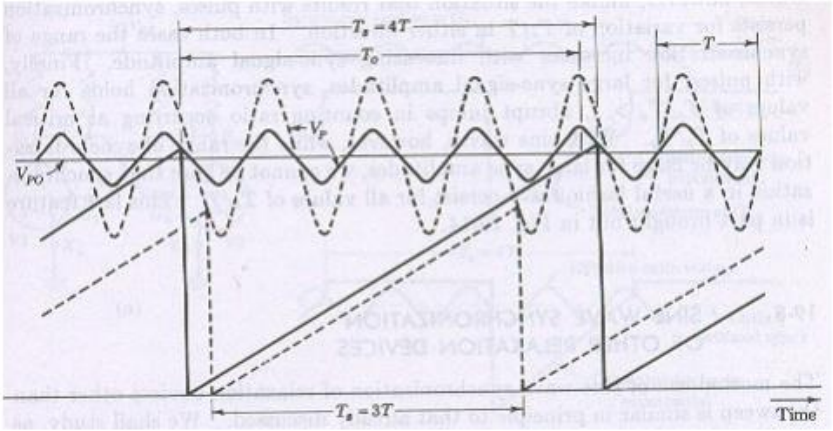


Figure The sweep circuit used as a counter. Illustrating the change in counting ratio with sync-signal amplitude.

Principle just large enough to cause 1:1 synchronization. The actual sweep waveform consists of alternate long and short sweeps.

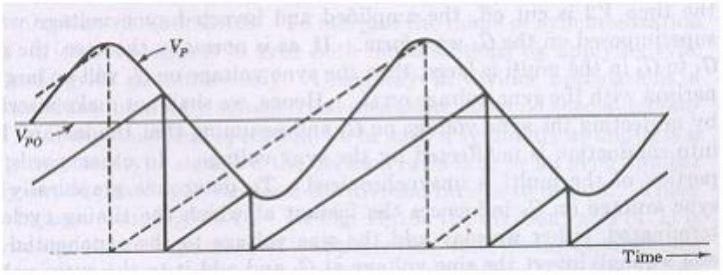


Figure Illustrating a possible result of excessive amplitude of the sync signal in a sweep

Sampling gates

Introduction:

A sampling gate is a transmission circuit in which the output is an exact reproduction of an input waveform during a selected time interval and is zero otherwise. The time interval for transmission is selected by an externally impressed signal which is called the gating signal or the control signal. These sampling gates basically of two types, one is called a unidirectional gate which allows signal of only one polarity to the output terminals and the other is a bidirectional gate which allows transmission of both positive and negative signals.

Sampling gate is a transmission circuit that faithfully transmits an input signal to the output, but only a for a selected time duration decided by an external signal, called a gating signal which is normally rectangular in shape. As shown in fig.

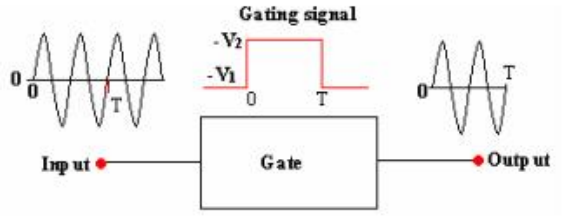


Fig. Sampling gate

The input appears at the output without distortion but is available for a time duration T and afterwards the signal is zero.

The sampling gates can be of two types.

(i) Unidirectional gates: These gates transmit signals of only one polarity.

(ii) Bidirectional gates: These gates transmit bidirectional signals (positive and negative signals).

Principle of operation of a linear gate:

Linear gates can use (a) a series switch or (b) a shunt switch fig

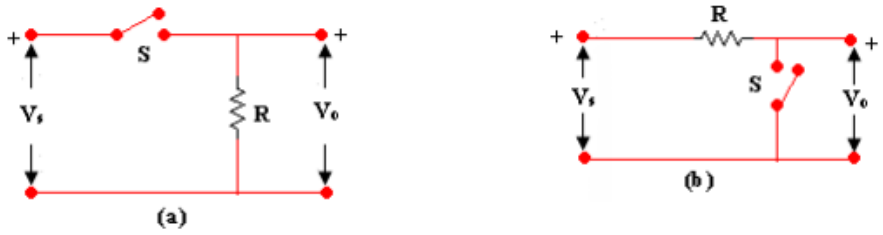


Fig. Linear gates

In (a) the switch closes for transmitting the signal whereas in (b) the switch is open for transmission to take place.

Unidirectional diode gate:

In order to transmit positive pulses the unidirectional gate shown in fig. below can be used.

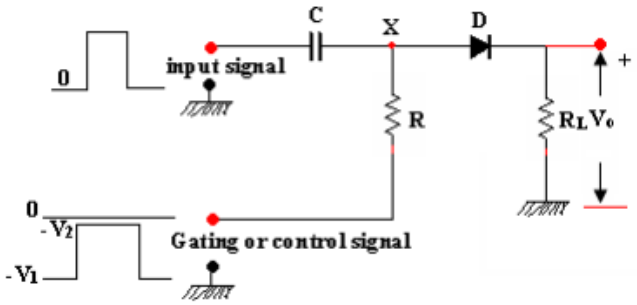


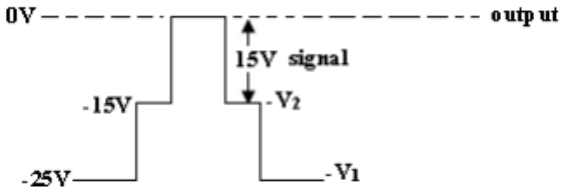
Fig. Unidirectional gate

The gating signal is also known as control pulse, selector pulse or an enabling pulse. It is a negative signal, the magnitude of which changes abruptly between $-V_2$ and $-V_1$.

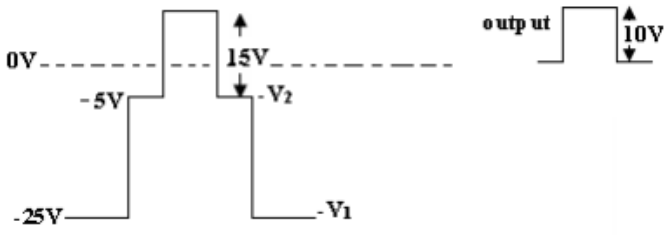
Consider the instant at which the gate signal is $-V_1$ which is a reasonably large negative voltage. Even if an input pulse is present at this time instant, the diode remains OFF as the input pulse amplitude may not be sufficiently large so as to forward bias it. Hence there is no output.

Now consider the duration when the gate signal has a value $-V_2$ and when the input is also present (coincidence occurs).

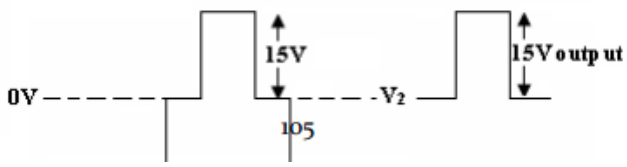
(i) for example, $-V_1 = -25V$, $-V_2 = -15V$ and the signal amplitude is 15V.



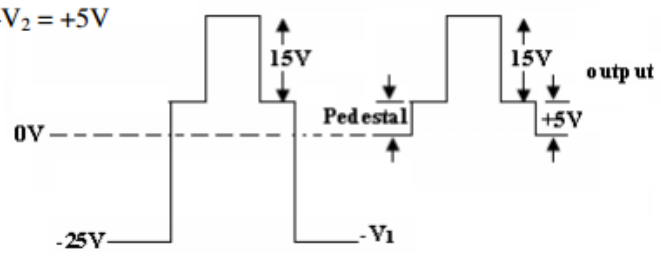
(i) Now let $-V_2$ be -5V



(ii) $-V_2$ now is 0V



(iii) Let $-V_2 = +5V$



The output of the gate changes by adjusting $-V_2$ and in the last case it is seen that the output is superimposed on a pedestal of 5V. Thus the output is influenced by the control signal.

But, for the gate signal RC network behaves as an integrator. Hence the gate signal is not necessarily a rectangular pulse but rises and falls with a time constant RC. As a result there is a distortion in gate signal. But if the duration of the input signal is much smaller than the duration of the gate, the output is a sharp pulse as desired.

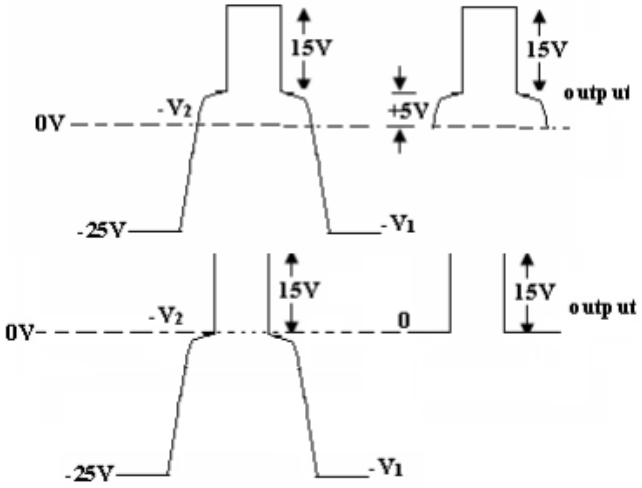


Fig. distortion in the gate signal

A unidirectional diode coincidence gate:

A unidirectional diode coincidence gate is shown below.

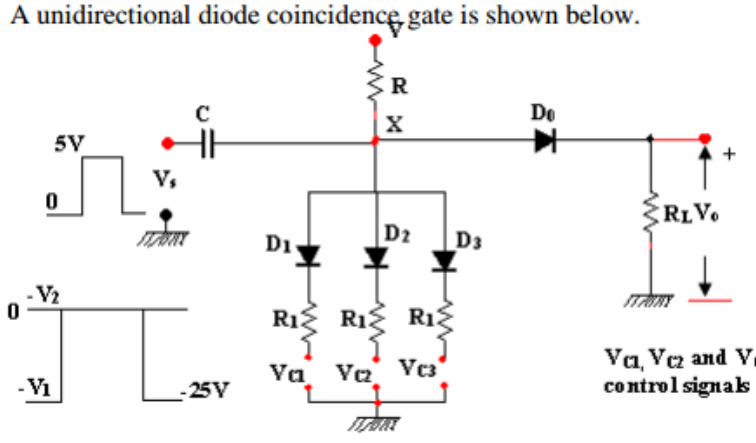


Fig. A unidirectional diode AND gate

When any of the control voltages is at $-V_1$, point X is at a large negative voltage, even if the input pulse V_s is present., D_0 is reverse biased. Hence there is no signal at the output.
When all the control voltages, on the other hand, are at $-V_2$, if an input signal V_s is present, D_0 is forward biased and the output is a pulse of 5V. Hence this circuit is a coincidence circuit or AND circuit.

Bidirectional sampling gates:

Till now we have considered gates that pass only unidirectional signals. Bidirectional sampling gates transmit bidirectional signals. These gates can be derived using diodes, transistors, FETS etc. A single transistor bidirectional sampling gate is shown in fig.

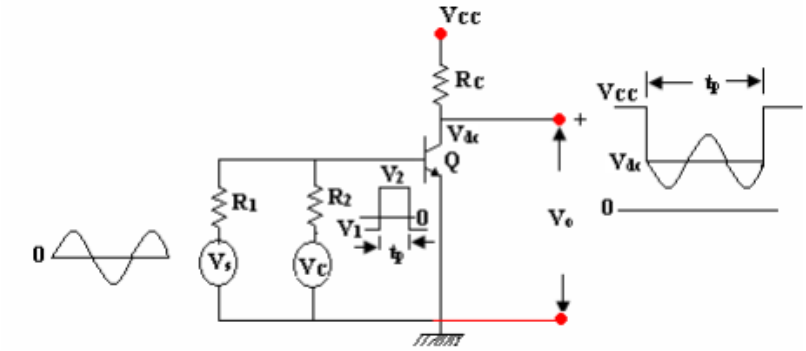


Fig. Bidirectional transistor gate

The control signal and the input are applied to the base of Q. The control signal is a pulse whose amplitude varies between V_1 and V_2 and has a duration t_p sufficient enough for signal transmission. As long as V_C is at the lower level V_1, Q is OFF and at the output we have only a dc voltage V_{CC}. However, when V_C is at its upper level V_2, Q is ON for the duration t_p and if the input signal is present, is amplified and transmitted to the output with phase inversion but referenced to a dc voltage V_{dC}. At the end of t_p, Q is again OFF and the dc voltage at its collector jumps to V_{CC}. Thus the signal is transmitted when the gating signal is at V_2.

Following figure shows another bidirectional transistor gate where two devices Q_1 and Q_2 are used and the control signal and the input signal are connected to two separate bases.

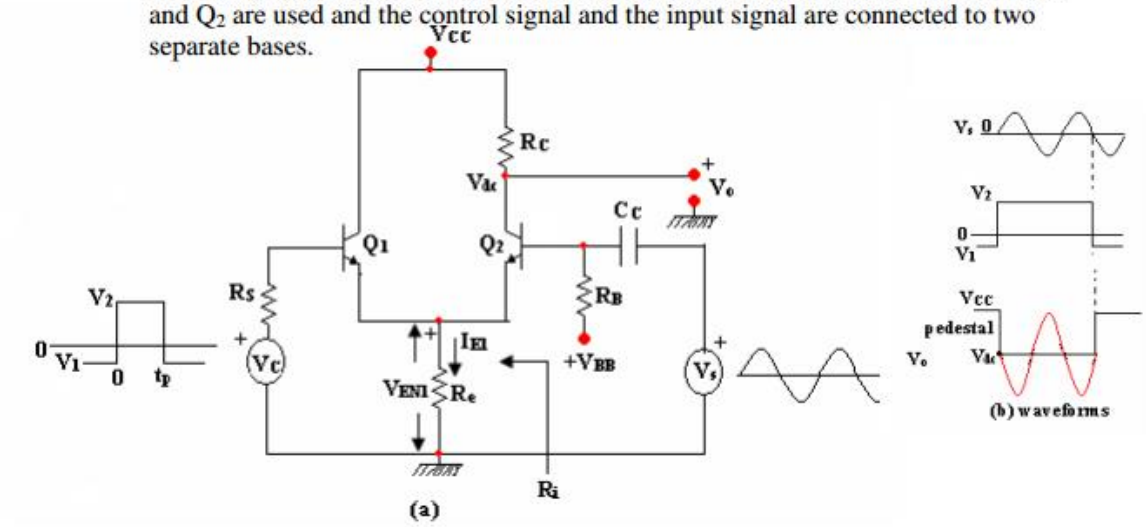


Fig. Bidirectional gate using two transistors

Let the control voltage be at its upper level, V_2 then Q_1 is ON and there is sufficient emitter current I_{E1} which results in V_{EN1} across R_e. And if this voltage is sufficient enough to reverse bias the base emitter diode of Q_2, then Q_2 is OFF. There is no signal output. When the gating signal is at its lower level V_1, Q_1 is OFF and Q_2 operates in the active region and can operate as an amplifier and if an input signal is present, there is an amplified output V_o. Presence of R_e increases the input resistance R_{i2} and thus signal source is not loaded.

From the waveforms shown in fig.(b) it is seen that the output is V_{CC} when Q_2 is OFF. When the gating signal drives Q_1 OFF and Q_2 ON, the dc voltage at the collector of Q_2 falls to V_{dc} (a voltage smaller than V_{CC}) and during the period of the gating signal, the signal is amplified by Q_2 and is available at the output. Again at the end of the gating signal Q_2 goes OFF and V_o jumps to V_{CC}. Hence the signal is superimposed on a pedestal.

A circuit arrangement that reduces this pedestal is shown in fig.

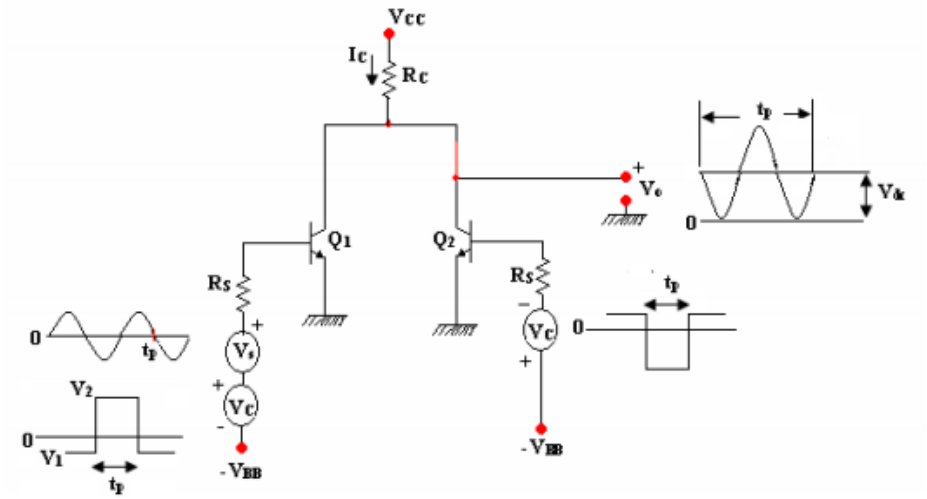
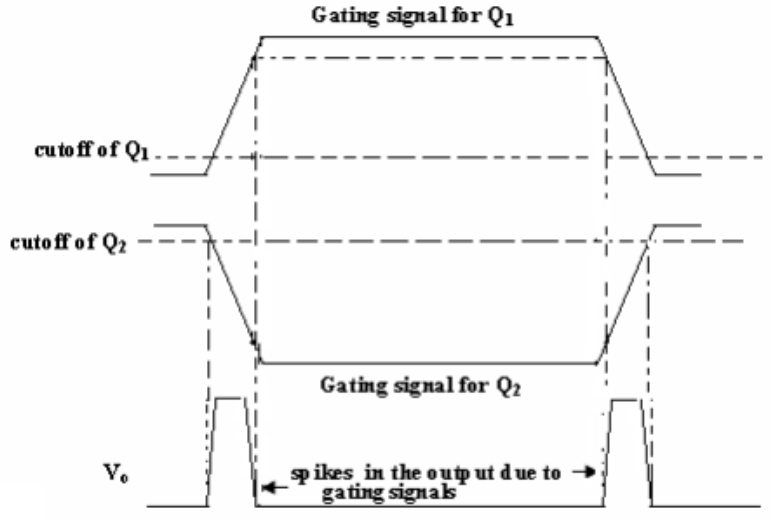


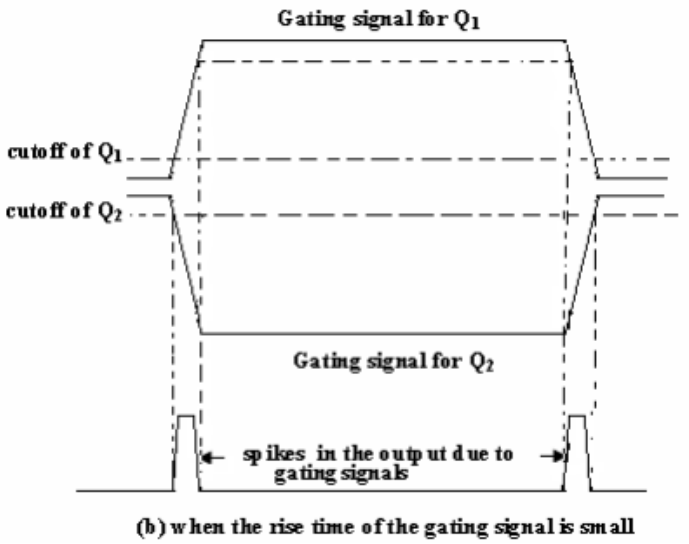
Fig. Circuit that minimizes the pedestal

The control signal applied to the base of Q_2 is of opposite polarity to that applied to the base of Q_1. When the gating signal connected to Q_1 is negative, Q_1 is OFF and at the same time the gating signal connected to Q_2 drives Q_2 ON and draws current I_C. As a result there is a dc voltage V_{dc} at the collector. But when the gate voltage at the base of Q_1 drives Q_1 ON, Q_2 goes OFF. But during this gate period if the input signal is present, it is amplified and is available at the output, with phase inversion. But the dc reference level practically is V_{dc}. As such the pedestal is either eliminated or minimized.

If the gating signals are not ideal pulses but have a finite risetime, these may give rise to spikes in the output.fig.



(a) when the rise time of the gating signal is large



(b) when the rise time of the gating signal is small

Spikes in the output when gating signals are not perfect pulses

If the gate pulse is a large negative voltage when compared to the V_{BE} of the devices when in active region, then the base of that transistor is far below cutoff. Now when the gate voltage is present Q_2 goes OFF before Q_1 goes ON. Similarly, at the end of the gating signal Q_1 goes OFF before Q_2 goes ON. As a result the gating signals themselves give rise to spikes in the output. If the rise time of the gating signal is large, these spikes are of larger duration where as if the rise time of the gating signal is small, these output spikes are of smaller duration. If the rise time of the gating signal is small when compared to the duration of the gate, these spikes will not cause distortion of the signal and hence are not objectionable.

BIDIRECTIONAL DIODE GATE

A bidirectional diode gate is shown in fig.(a).

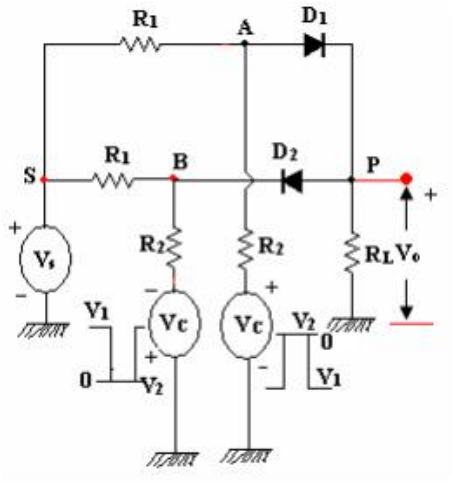


Fig.(a) Bidirectional diode gate

The above circuit is redrawn in fig.(b)

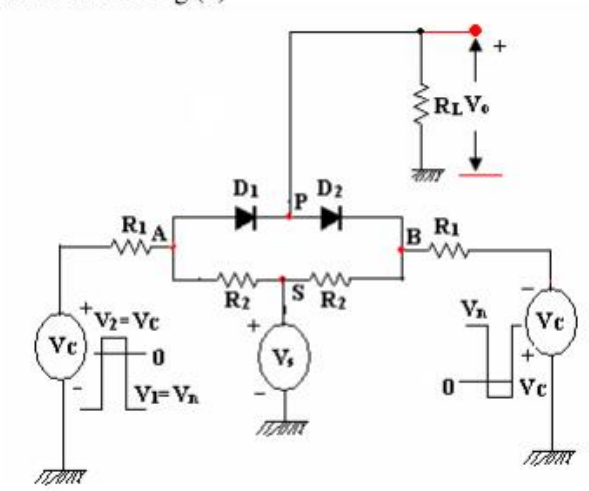
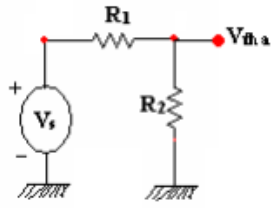


Fig.(b) Bidirectional gate in the form of a bridge circuit

When the control signals are at V_1, D_1 and D_2 are OFF, no input signal is transmitted to the output. But when control signals are at V_2, diode D_1 conducts if the input is positive pulses and diode D_2 conducts if the input is negative pulses. Hence these bidirectional inputs are transmitted to the output. This arrangement eliminates pedestal, because of the circuit symmetry.

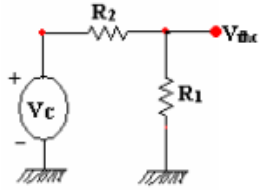
Thevinising the circuit ,fig.(b), at A, the Thevinin voltage source magnitude due to V_s is (shorting V_C source)



$$V_{ths} = \frac{R_2}{R_1 + R_2} V_s$$
$$= \alpha V_s$$

$$where \quad \alpha = \frac{R_2}{R_1 + R_2} \quad and \quad R_{th} = R_1 // R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

Similarly, thevinising the circuit in fig.8.16 at B, the Thevinin source due to V_C is (shorting V_s).



$$V_{thc} = \frac{R_1}{R_1 + R_2} V_C$$

$$R_{thc} = R_1 // R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{thc} = (1 - \alpha) V_C = (1 - \frac{R_2}{R_1 + R_2}) V_C = \frac{R_1}{R_1 + R_2} V_C$$

Redrawing the circuit and replacing the diode by its linear model we have.

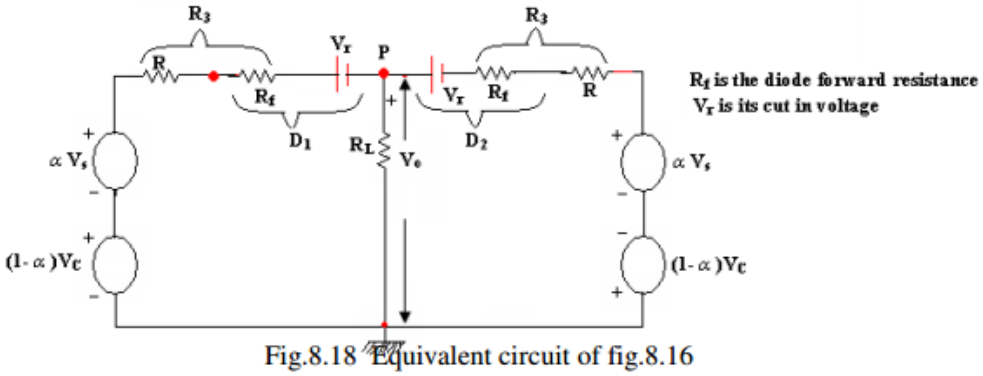
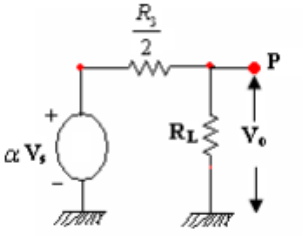


Fig.8.18 Equivalent circuit of fig.8.16

$R_3 = R_f$

Now define the **gain of the transmission gate A,** as the ratio of $\frac{V_o}{V_s}$ during transmission period. The control and small diode voltages donot contribute to any current in R_L.

The open circuit voltage between P and ground is αV_s and the Thevinin resistance is $\frac{R_3}{2}$.



$$V_o = \alpha V_s \frac{R_L}{R_L + \frac{R_3}{2}}$$

$$A = \frac{V_o}{V_s} = \alpha \frac{R_L}{R_L + \frac{R_3}{2}}$$

$$But\ \alpha = \frac{R_2}{R_1 + R_2}$$

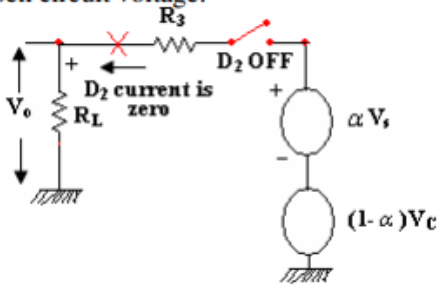
$$\therefore A = \frac{R}{R_1 + R_2} \times \frac{R_L}{R_L + \frac{R_3}{2}}$$

Minimum control voltage V_C(min) required to keep diodes D_1 and D_2 in forward bias:

Suppose that the signal voltage attains a maximum voltage V_s. Then tthere is a minimum control voltage that is required to ensure that both diodes will continue to conduct. Consider only gating signals are present. The amplitude and polarity of the gating signals are such that both the diodes D_1 and D_2 conduct, and equal currents flow in these two diodes. Under such conditions, the net voltage drop is zero and there is no pedestal.

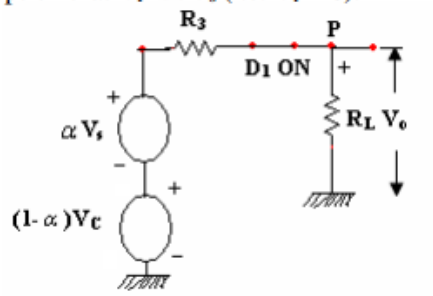
Let V_s be positive signal. As the amplitude of the signal goes on increasing, the current in D_1 goes on increasing and that in D_2 goes on decreasing. As V_s increases further, the current in D_2 becomes zero (i.e. D_2 is OFF). Thus there is a minimum control voltage V_C that will keep both the diodes ON. To calculate this $V_{C(min)}$, let D_2 be just stopped conducting i.e. the diode current has become zero, the drop across R_3 is zero. Therefore the output voltage across R_L is the open circuit voltage.

V_o when D_2 is OFF



$$V_o = [\alpha V_s - (1-\alpha)V_C]$$

Now, calculating the output due to the left hand side signal source V_s and control signal $(1-\alpha)V_C$, with the assumption that $V_r << V_s$ (i.e. $V_r \approx 0$).



V_o when D_1 is ON

$$V_o = [\alpha V_s - (1-\alpha)V_C]\frac{R_L}{R_L + R_3}$$

Above two equations represent V_o, hence

$$[\alpha V_s - (1-\alpha)V_C]\frac{R_L}{R_L + R_3} = \alpha V_s - (1-\alpha)V_C$$

$$\alpha V_s(1 - \frac{R_L}{R_L + R_3}) = (1-\alpha)V_C\left[\frac{R_L}{R_L + R_3} + 1\right]$$

$$\alpha V_s(\frac{R_L}{R_L + R_3}) = (1-\alpha)V_C\left[\frac{R_L}{R_L + R_3} + 1\right]$$

$$\alpha V_s R_3 = (1-\alpha)V_C(R_3 + 2R_L)$$

$$\alpha = \frac{R_2}{R_1 + R_2} \quad \text{and} \quad 1-\alpha = 1 - \frac{R_2}{R_1 + R_2} = \frac{R_1}{R_1 + R_2}$$

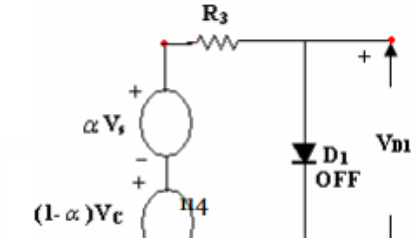
$$\frac{R_2 R_3}{R_1 + R_2} V_s = \frac{R_1}{R_1 + R_2}(R_3 + 2R_L)\, V_C$$

$$V_{C(min)} = \frac{R_2}{R_1} \times \frac{R_3}{R_3 + 2R_L} V_s$$

$V_{C(min)}$ decreases with increasing R_L.

Minimum control voltage $V_{n(min)}$ to ensure that D_1 and D_2 are off

To calculate the minimum control voltage $V_{n(min)}$ that is needed to keep D_1 and D_2 OFF when no sampling takes place consider the voltage at point P is zero i.e. at ground potential.



V_{D1} = Voltage across D_1 = $[\alpha V_s - (1-\alpha)V_C]$

If V_n is the magnitude of V_C at the lower level.

$V_{D1} = [\alpha V_s - (1-\alpha)V_n]$

For D_1 to be OFF, V_{D1} must be either zero or negative. If V_{D1} is zero

$[\alpha V_s - (1-\alpha)V_n] = 0$

$$V_n = V_{n(\min)} = \frac{\alpha V_s}{1-\alpha}$$

$$\frac{\alpha}{1-\alpha} = \frac{R_2}{R_1}$$

$$\therefore V_n(\min) = \frac{R_2}{R_1} V_s$$

In practice $V_{C(min)}$ and $V_{n(min)}$ are larger by 25%.

Four diode gate:

Following are the disadvantages with two diode gate.

(i) there is an appreciable attenuation of the signal since A is small,

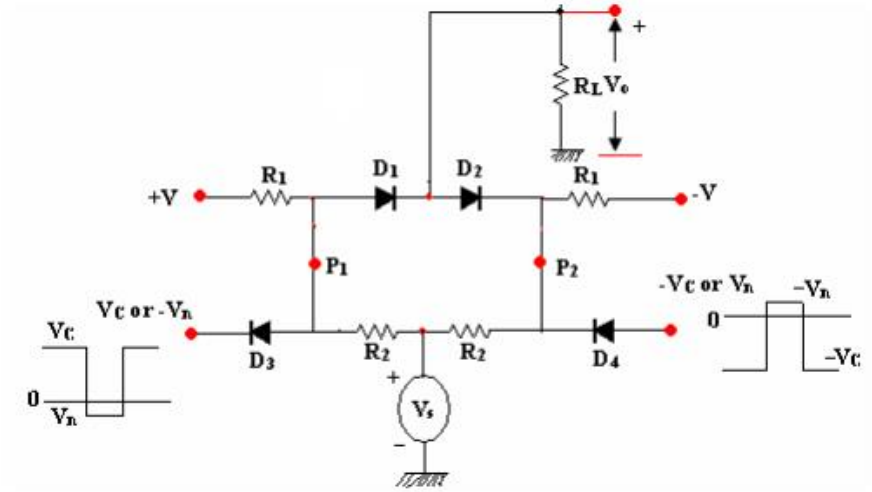
(ii) the two control voltages V_C and $-V_C$

(iii) should be equal in magnitude and opposite in polarity, failing which there could be a pedestal in the output and

(iv) $V_{n(min)}$ can be appreciably large.

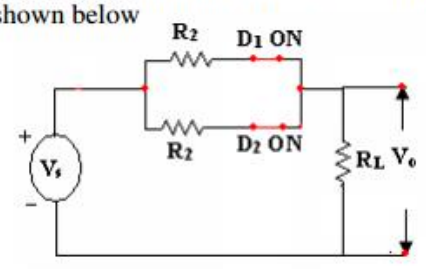
The above limitations can be overcome in a four diode gate .

Here two balanced dc voltages +V and –V are used



A Four diode gate

When the control voltages are V_C and $-V_C$, D_3 and D_4 are reverse biased and are OFF. However, D_1 and D_2 are ON because of +V and –V. The signal is connected to the load through R_2 and the conducting diodes as shown below



When the signal is transmitted, as D_3 and D_4 are OFF, even if there is a slight imbalance in the two control voltages $+V_C$ and $-V_C$, there is no pedestal at the output.

On the otherhand, when the control voltages are at V_n and $-V_n$ respectively, D_3 and D_4 conduct. As a result D_1 and D_2 are OFF. Now the output is zero.

When D_3 and D_4 are OFF, the circuit is similar to a two diode gate and A is the same

Also the minimum value of voltage V_{min} is the same as $V_{C(min)}$ except for the fact that V_C and $-V_C$ are replaced by V and –V.

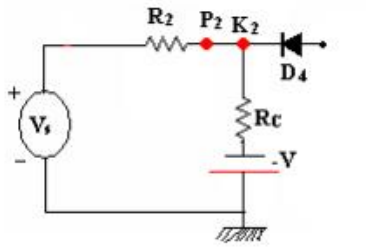
$$\therefore V_{min} = \frac{R_1}{R_2} \times \frac{R_3}{R_3 + 2R_L} \times V_s$$

To calculate $V_{C(min)}$, if $R_f << R_L$, for a positive V_s the voltage at P_1 is AV_s. If D_3 is to be OFF. V_C must at least be equal to AV_s.

ie. $V_{C(min)} \approx AV_s$

$V_{n(min)}$ is calculated to satisfy the condition that D_2 is OFF and D_4 is ON.

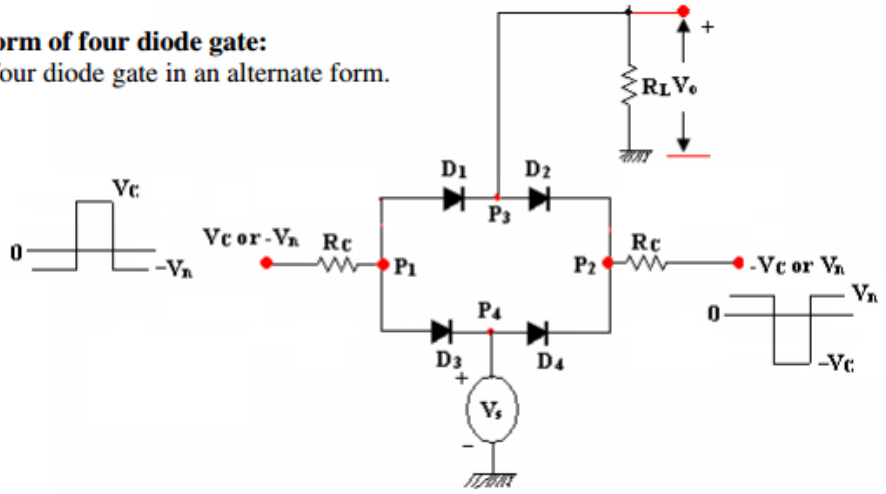
Calculating the voltage at the cathode of D_4 due to sources –V and V_s using the superposition theorem



The minimum voltage $V_{n(min)}$ should atleast be equal to V_{K2}

$$\therefore V_{n(min)} = V_s \times \frac{R_C}{R_2 + R_C} - V \times \frac{R_2}{R_2 + R_C}$$

Alternate form of four diode gate:
Consider a four diode gate in an alternate form.



other form of four diode gate

When the control signals are V_C and $-V_C$, D_1,D_2,D_3 and D_4 are ON.
Consider only V_C and $-V_C$ sources ($V_s = 0$),

In this arrangement, $\frac{V_C}{R_C}$ is the total current and $\frac{V_C}{2R_C}$ is the current in each arm.

Now,when considering the signal source V_s only($V_C = 0$),
The voltages V_C and $-V_C$ depend on the amplitude of V_s of the signal, that satisfies the condition that all the diodes are conducting i.e. current flows in the forward direction.
The net current in the diodes is due to the sources V_C and V_s.

The current in each diode due to the V_C sources is $\frac{V_C}{2R_C}$ and this is a forward current.

On the otherhand, the current due to V_s source flows in the reverse direction in D_3 and D_2. The reverse current in D_3 is $\frac{V_s}{R_C}+\frac{V_s}{2R_L}$ and that in D_2 is $\frac{V_s}{2R_L}$. Thus the reverse current in D_3 is larger than the reverse current in D_2.
For the diode D_3 to be conducting, the forward current should be greater than the reverse current. We can, therefore, arrive at the minimum value of V_C($V_{C(min)}$), when the forward current is equal to the reverse current.

$$\frac{V_C}{2R_C}=\frac{V_s}{R_C}+\frac{V_s}{2R_L}$$

$$V_{C(min)} = 2V_s + \frac{R_C}{R_L}\times V_s = V_s(2+\frac{R_C}{R_L})$$

If R_f and R are much smaller than R_C or R_L. Then P_1,P_2,P_3 and P_4 are all at ground potential.
If P_1 is approximately at ground potential

$$I_1 = \frac{V_C}{R_C}$$

v

$$I = I_1 \times \frac{R_f + \frac{R}{2}}{R_f + R_f + \frac{R}{2}}$$

$$= \frac{V_C}{R_C} \times \frac{R_f + \frac{R}{2}}{2R_f + \frac{R}{2}}$$

$$= \frac{V_C}{R_C} \times \frac{2(2R_f + R)}{2(4R_f + R)}$$

$$= \frac{V_C}{2R_C}\left[\frac{4R_f + 2R)}{(4R_f + R)}\right]$$

$$= \frac{V_C}{2R_C}\left[\frac{1 + \frac{R}{2R_f}}{1 + \frac{R}{4R_f}}\right]$$

$$I \approx \frac{V_C}{2R_C}\left[\frac{1}{1 + \frac{R}{4R_f}}\right]$$

The larger reverse current in D_3 (I_2) is due to V_s (when $V_C = 0$)

$$I_2 = \frac{V_S}{R_C} + \frac{V_S}{2R_L}$$

For V_C to be $V_{C(min)}$, the forward current due to V_C (I) and the reverse current due to V_s (I_2) must just be equal.

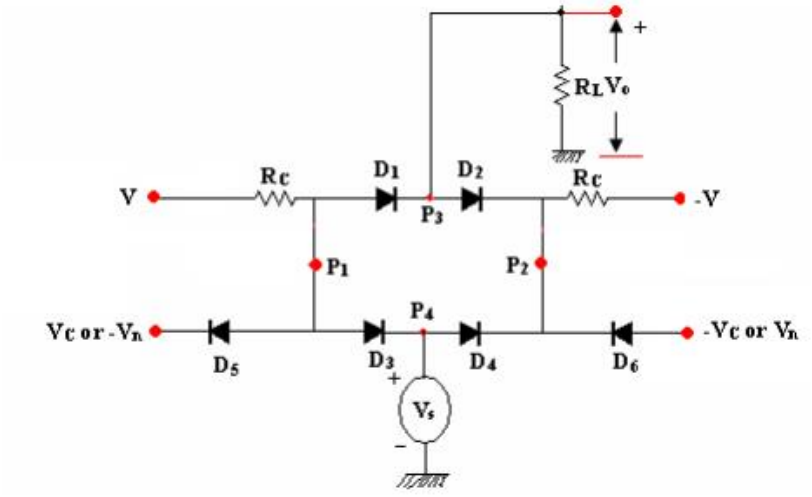
$$\frac{V_S}{R_C} + \frac{V_S}{2R_L} = \frac{V_C}{2R_C}\left[\frac{1}{1 + \frac{R}{4R_f}}\right]$$

$$\frac{V_{C(min)}}{2R_C} = \left(\frac{V_S}{R_C} + \frac{V_S}{2R_L}\right)\left(1 + \frac{R}{4R_f}\right)$$

$$V_{C(min)} = \left(2V_S + V_S \times \frac{R_C}{R_L}\right)\left(1 + \frac{R}{4R_f}\right)$$

$$\therefore\ V_{C(min)} = V_S\left(2 + \frac{R_C}{R_L}\right)\left(1 + \frac{R}{4R_f}\right)$$

Six diode gate: A six diode gate is shown in fig.



A six diode gate

This is similar to the four diode gate shown earlier except that two more diodes D_5 and D_6 are included.

When no signal is transmitted D_5 and D_6 conduct while D_1 to D_4 remains OFF.

During transmission, D_5 and D_6 are OFF and this six diode gate is equivalent to the four diode gate seen earlier.

If the diodes D_5 and D_6 are remain OFF for a signal amplitude V_s, then

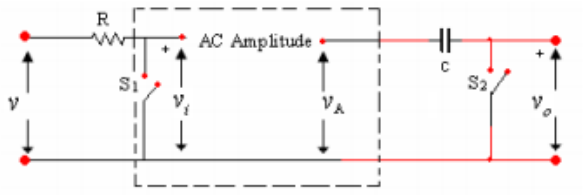
$V_{C(min)} = V_s$

The minimum required value of V_n is $V_{n(min)}$ and is equal to V_s since the transmission diodes D_1 to D_4 will not conduct unless V_s exceeds V_n.

Hence $V_{n(min)} = V_s$

Chopper stabilized amplifier:

Sometimes it becomes necessary to amplify a signal v that has very small dv/dt and that the amplitude of the signal itself is very small, typically of the order of millivolts. Neither, ac amplifiers using large coupling condensers nor dc amplifiers with the associated drift would be useful for such an application. A chopper stabilized amplifier employing sampling gates can be a useful choice in such a applications



Chopper stabilized amplifier

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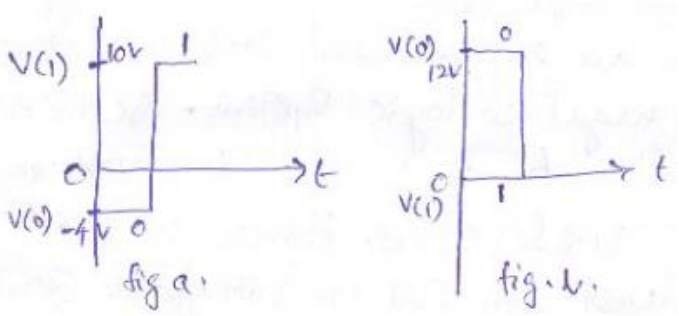
LOGIC CIRCUITS

Introduction ;

In large scale digital systems such as in a digital computer, data processing, control or digital communication system a few basic operations are needed. These are four circuits known as OR, AND, NOT and flip-flop. These are called logic gates or circuits because their operations uses logic algebra or Boolean algebra.

Logic System :

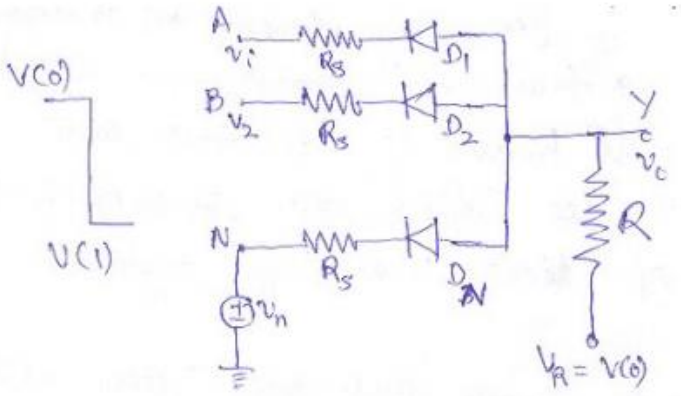
In a de-or level-logic system a bit is implemented as one of two voltage levels as shown below.



- In fig (a) more positive voltage is the level 1 and the other is the level 1 and the other is the level 0. this is called as de-positive logic.
- In fig(b) more negative voltage state is represented with 1 and more positive with 0, which is known as negative logic.
- In a dynamic or pulse logic system of bit is recognized by the presence or absence of a pulse.
- In a dynamic positive logic system, positive pulse indicates 1 and its absence or no pulse signifies 0.
- Similarly a negative pulse indicates 1 in a dynamic negative system and no pulse or absence specifies 0.

OR gate :

The output of an OR assumes 1 state if any one of the inputs assumes 1 state. The N input logic circuit with output y is represented as shown below. Truth table for 2 input circuit is mentioned to understand simply.



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

In the circuit, since the diodes only are used, it is called diode logic (DL) system. Here upper and lower voltages are represented with $V(0)$ and $V(1)$ respectively, it is a negative logic system. If all inputs are applied by $V(0)$, the the voltage across each diode is $V(0)-V(0)=0$. Hence no diode is forward biased by at least the cut voltage V_γ and none of the diode conducts. Therefore the output voltage is $V_0 = V(0)$ and so the gate is said to be in the 0 state.

If one of the inputs, say A, is changed to 1 state and for negative logic system, the level $V(1)$ makes that diode forward bias. So diode D_1 conducts and hence current flows in the resistance R. Therefore the output is given by

$$V_0 = V(0)[V(0)-V(1)-V_\gamma]\frac{R}{R+R_s+R_f}$$

Where R_f is the forward resistance and R_s is the source resistance.

As R_f and R_s are smaller than R,

The above expression can be reduced to

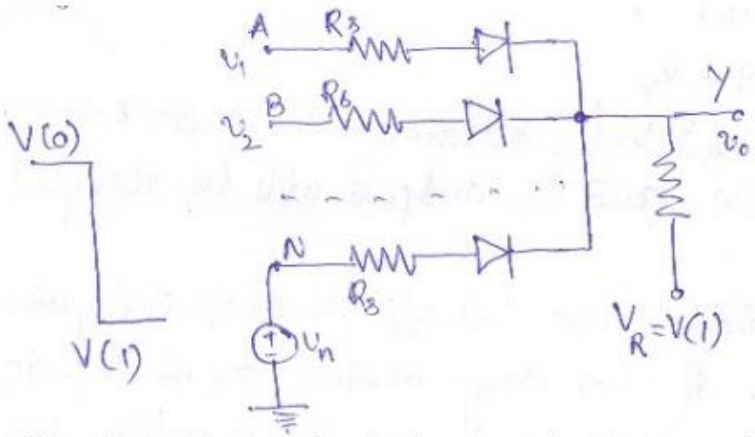
$$V_0 = V(1) + V_\gamma$$

So the output voltage exceeds the more negative level $V(1)$ by V_γ that means output voltage is smaller by V_γ than the change in input voltage. If for any reason the level $V(1)$ is not identical for all inputs then the most negative value of $V(1)$ (for negative logic) appears at the output. A positive logic OR gate can also be designed but this is same as above circuit except all diodes must be reversed.

AND gate :

Definition :

The output an AND assumes the 1 state if and only if all the inputs assume the 1state. A diode (DL) configuration for a negative AND gate is shown below with truth table for 2 inputs.



inputs		output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

To understand the operation simply, assume that all source resistances R_s are zero and that the diodes are ideal. If any input is at the 0 level $V(0)$, the diode connected to this input conducts and the output is clamped at the voltage $V(0)$ or $Y = 0$.

If all the inputs are at the 1 level $V(1)$, then all diodes are reverse biased and $V_0 = V(1)\ or\ y = 1$.

Taking source resistance R_s and diode forward resistance R_f into account, we can determine the output of the circuit for positive logic system. Assume in inputs out of n are at $V(1)$ and hence in diodes are reverse biased. The remaining n-m diodes conduct

and hence the effective circuit of these diodes in parallel consists of $(R_S + R_f)/(n-m)$ in series with a voltage V_γ. Then the output is

$$V_0 = V(1) - [V(1) - V(0) - V_\gamma] \frac{R}{\left[R + \frac{(R_S + R_f)}{n-m}\right]}$$

From this, if all inputs are at 1 state, i.e., $m = n$,

The output is clamped at a value V_γ above the $V(0)$ level.

i.e., $V_0 = V(0) + V_\gamma$

In the circuit if $V_R > V(1)$, all diodes conduct when all inputs are at $V(1)$, and the output will be clamped to $V(1)$.

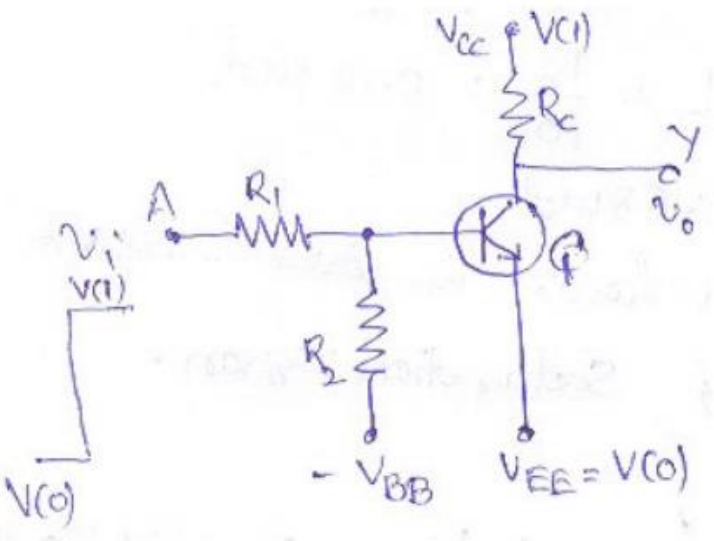
If $V_R = V(1)$, all diodes are cut off the output impedance is high (equal to R). If for any reason all the inputs are not at the same upper level $V(1)$, then the output will be equal $V(1)_{max}$.

Similarly, if $V_R < V(1)$, and all the inputs are at 1, then all diodes will be cut off upon coincidence and the output will rise to the voltage V_R.

NOT or INVERTER Circuit

The NOT logic circuit has a single input and single output. It is defined as the output of a NOT circuit takes on the 1 state if and only if the input does not take on the 1 state.

The following transistor circuit performs the logic NOT operation in the dc positive logic system.

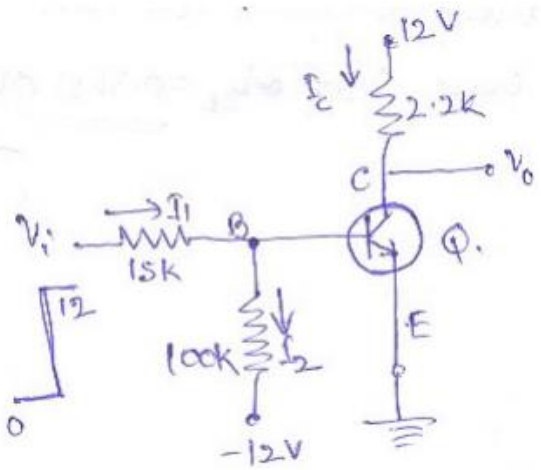


- If the input is low, $V_i = V(0)$, then the parameters are chosen so that in Q is OFF and hence $V_0 = Vce = V(1)$.

- When the input is changed to high state i.e., $V(1)$, then the circuit parameters are picked so that the transistor Q is in saturation and then $v_0 = V_{EE} = V(0)$. Actually, the saturation voltage will be very low i.e., a few tentsa of a volt and that can be neglected.

Problem :

Find the output levels for input levels of 0 and 12V if the silicon transistor shown below has a minimum value of h_{FE} *of* 30.



Sol. Assume $V_{BEsat} = V_{CEsat} = 0V$, For $V_i = V(0) = 0V$. The open circuited base votlage V_B is

$$V_B = (-12)\frac{15}{15+100} = -1.56V$$

This makes the npn transistor cutoff. Since 0v is adequate for a silicon emitter junction.

Therefore Q is indeed in the cutoff

Hence $V_0 - 12V = V(1)$.

For $V_i = V(1) = 12V$.

To show the transistor in the saturation region, the minimum base fdsa current required for saturation is

$$(I_B)_{\min} = \frac{I_C}{h_{FE}}$$

$$\therefore I_C = \frac{12}{12.2} = 5.45mt; \qquad (I_B)_{\min} = \frac{5.45}{30} = 0.18mA$$

And $I_1 = \frac{12}{15} = 0.8mt; \qquad I_2 = \frac{12}{100} = 0.12mA$

$$\therefore I_B = -I_1 - I_2 = 0.8 - 0.12 = 0.68mt$$

That means $(I_B)_{\min} > I_B$ and hence the transistor is indeed in the saturation region.

$$\therefore v_0 = V_{CE} = 0$$

If we take the actual value of V_{BEsat} & V_{CEsat} as 0.7V & 0.3V respectively for a silicon transistor, then

$$I_C = \frac{12-0.3}{2.2} = 5.31mt; \qquad (I_B)_{\min} = \frac{5.31}{30} = 0.18mA$$

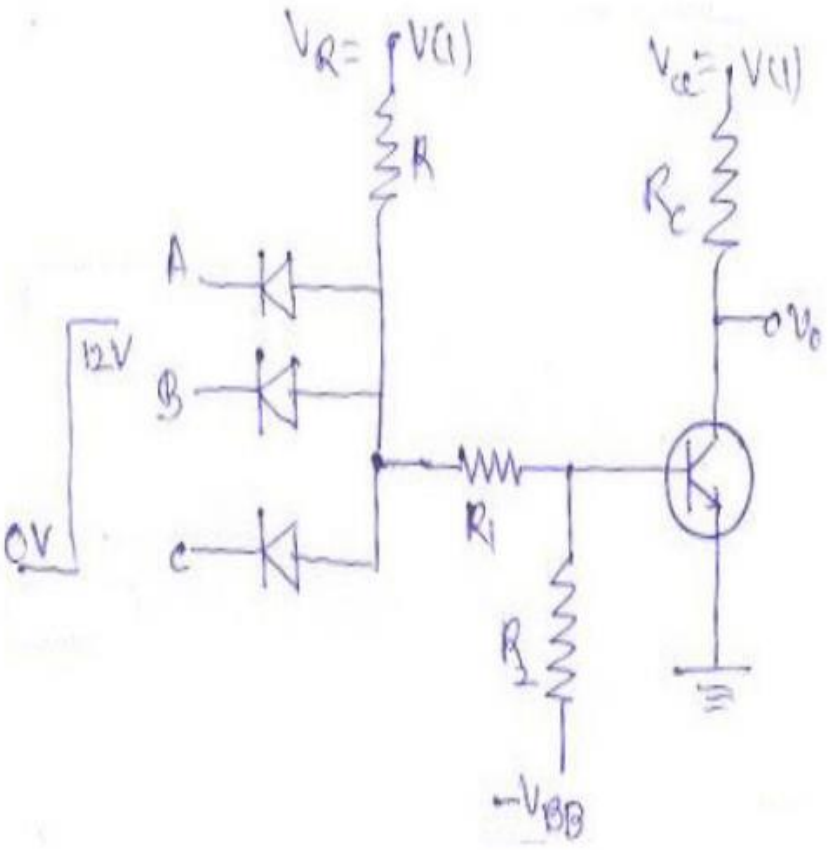
$$I_1 = \frac{12-0.7}{15} = 0.75mA \text{ and } I_2 = \frac{0.7-(-12)}{100} = 0.13mA$$

And $I_B = 0.75 - 0.13 = 0.62$ which is greater than $(I_B)_{\min}$

Hence the transistor with these values are also in the saturation region. Hence $V_0 = V_{CE} = 0.3V \cong 0V$

NAND Gate

A negation following an AND gate is called a NOT-AND or NAND gate. A positive NAND circuit is implemented by a cascade of diode AND and a transistor NOT as shown in the circuit. Truth table for two input NAND circuit is mentioned.



inputs		output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Similarly a NOR circuit can also be designed by cascading a diode NOT with a resistacne OR But the positive NAND gate is same as that of a negative NOR. Thse NAND and NOR circuits are involving with diodes and transistors, these are also called as Diode-Transistor logic (DTL) gates.

In the above DTL configurations, the same can be implemented by omitting the diodes. Then logic gates are called transistor resistor logic TRL or Resistor-Transistor Logic RTL. If these resistors are shunted with capacitors then they are called as Resistor-Capacitor-Transistor (RCTL) logic circuits.

NON-LINEAR WAVESHAPING - CLAMPING CIRCUITS

Introduction:

The establishment of extremity of positive or negative signal excursion at some reference level V_R is called Clamping. Clamping circuits introduce the dc component lost during transmission through a capacitive coupled network. Circuits that clamp the positive peak of the signal to zero level are called negative clampers and those that clamp the negative peak of the signal to zero level are called positive clampers. If a non-sinusoidal periodic signal is transmitted through a network having capacitive coupling, the dc component in the output is lost since the capacitor blocks the dc. If there arises the need once again that dc component is to be restored, this is done by a clamping circuit. A clamping circuit is, therefore, called a dc restorer or dc reinserter. As such, the output can be referenced to any arbitrarily chosen reference level.

The clamping circuit:

The circuit in fig.i) is the basic clamping circuit.

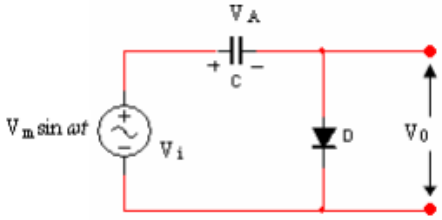


Fig.i) Negative Clamping circuit

As the input rises from 0 to V_m in the first quarter cycle fig.4.2a, C charges to V_m. During this period, $V_0 = 0$. i.e the output is zero for the first quarter cycle since D conducts . The input falls after the first quarter cycle. $V_i < V_m$, the charge on the capacitor. As a result the diode is reverse biased by a voltage $(V_i - V_m)$. Hence D is OFF .

$\therefore V_0 = V_i - V_m$ -------- 1

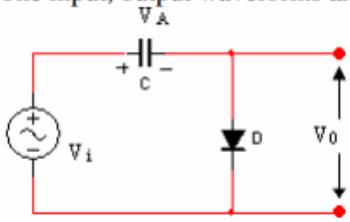
The voltage across C remains unchanged.

From equation .1----.If $V_i = 0$, $V_0 = -V_m$

And if, $V_i = -V_m$, $V_0 = -V_m - V_m = -2V_m$

During the next cycle, the positive peak of the output just reaches the zero level. Hence in the output, the positive peak is clamped to zero level and this is repeated for succeeding cycles.

The input, output waveforms are represented in fig.2



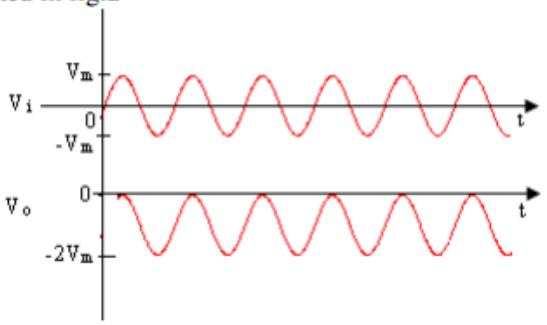


Fig.2 input – output waveforms of negative clamp

The input to this circuit is a sinusoidal with zero reference level. The output is referenced to $-V_m$ and the positive peak is clamped to zero.

When the input decreases, to clamp the positive peak to zero level, the voltage across the capacitor should change to the peak amplitude of the new input. But there is no discharge path for the capacitor to discharge. For this a resistance R is provided in shunt with the diode D fig.3

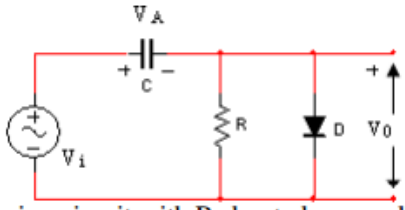


Fig.3 Clamping circuit with R shunted across diode D

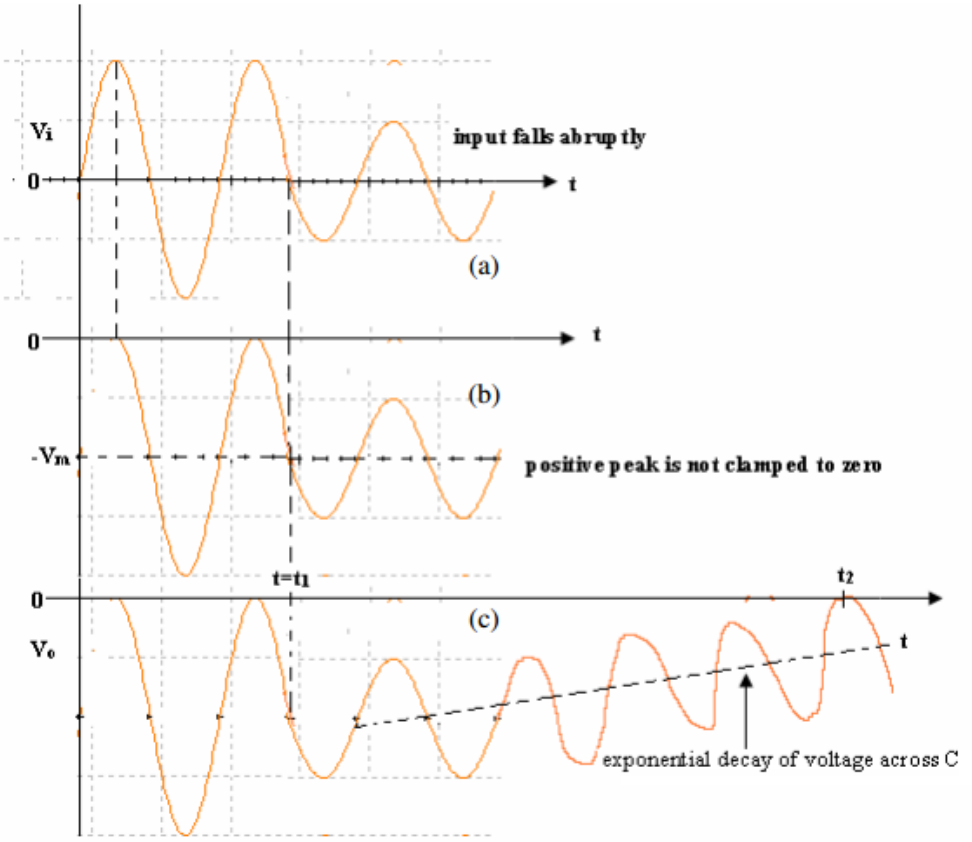


Fig.4 a) input b) Output when R = ∞ c) output with finite R

At $t = t_1$, if the input amplitude is abruptly reduced, as the voltage across the capacitor cannot change instantaneously, the positive peaks will not reach zero level. But now as the charge on C is going to discharge, as the voltage across the capacitor varies

exponentially with a time constant τ =RC, the output reaches zero level at t = t_2, the positive peak is again clamped to zero, after few cycles.

Fig.5 Output with expanded time scale in the neighborhood of a positive peak

In the vicinity of a positive peak D conducts and at t = t_2', V_0=0. If there were to be no diode, the output should have followed the dashed line with the peak at t = t_2. But because of the diode, the output in zero from t_2' to t_2 and in the subsequent cycles the positive peaks of the sinusoidal are clamped to zero.

Clamping circuit with diode and source resistances:

Consider now the internal resistance of the source, R_S.as shown in Fig.i)

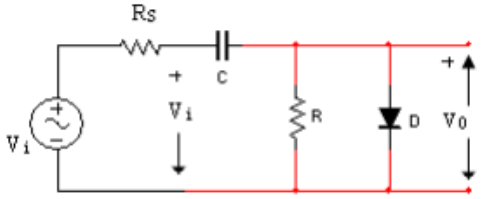


Fig.i) Clamping circuit with R_S

When the input is applied, the output reaches the steady-state value after a few cycles and the positive peaks are clamped to zero. consider the equivalent circuits

(i) When the diode is ON, fig.ii) and (ii) When the diode is OFF, Fig.iii)

(i) When the diode is ON

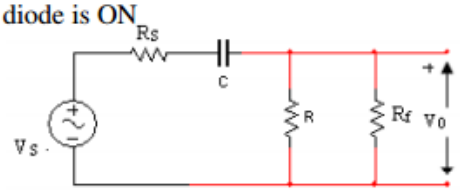
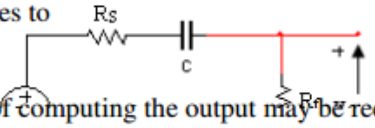


Fig.ii) Circuit when the diode is ON

As $R_f << R$, this circuit reduces to



This circuit, for the purpose of computing the output may be redrawn as fig.iv

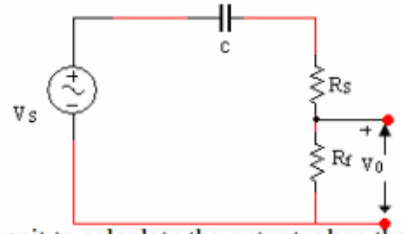
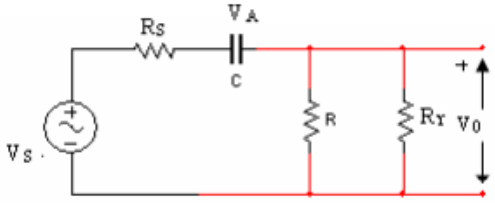


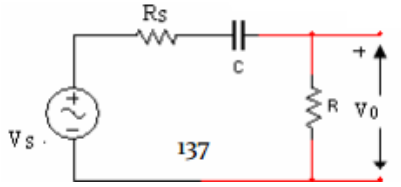
Fig.iv) Circuit to calculate the output when the diode is ON

(ii) when the diode is OFF

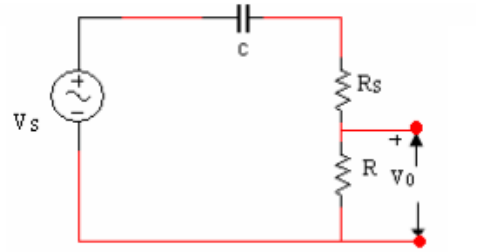


circuit when D is OFF

As $R_r >> R$, this circuit reduces to



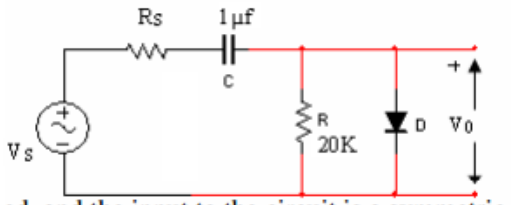
Again, for computing the output this circuit is redrawn as in Fig



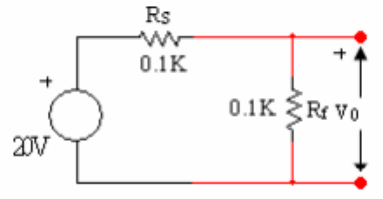
Circuit to calculate the output when the diode is OFF

Problem on clamping

To illustrate how the output reaches the steady-state in a negative clamp let us consider a specific example.



If initially C is uncharged, and the input to the circuit is a symmetric squarewave of whose amplitude varies from 0 to 20V. When the diode is conducting using the circuit of Fig.4.7(a).



$$V_0(0+) = 20V \times \frac{0.1K}{0.1K + 0.1K} = 10V$$

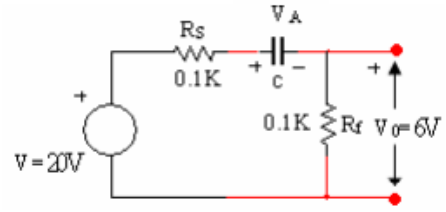
When the input abruptly jumps by 20V, the output jumps by 10V . As the input is constant during the period 0 to T/2, the output decays exponentially with the time constant

$\tau = (R_f + R_s)C = 0.2 \times 10^3 \times 1 \times 10^{-6} = 0.2\text{msec}$

Let f = 5KHZ, $T = \frac{1}{f} = 0.2$ msec

T/2 = 0.1msec, T = τ

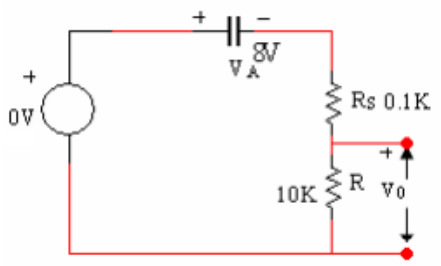
Hence ,$V_0(T/2) = 10\,e^{\frac{-T}{2\tau}} = 10\,e^{\frac{-1}{2}} = 6V$

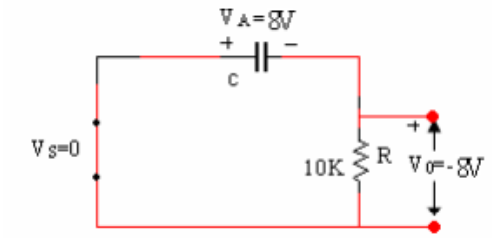


The voltage across capacitor V_A is

= 20V – (6V+6V) = 8V

At t = T/2, the input falls to 0V, the diode is OFF and the equivalent circuit of Fig.4.8a is used





The output falls to -8V suddenly. As the input has remained constant from T/2 to T, the output decays with time constant $\tau' = 10K \times 1\mu F = 10msec$

T/2 is 0.1msec and $\tau' = 10msec$

$T/2 << \tau'$

Hence there is no appreciable decay of the output

$$V_0(T) = -8\, e^{\frac{-T}{2\tau'}} \approx -8V$$

i.e. the output remains constant. In the interval T/2 to T, as the output has remained constant, the voltage across the capacitor has remained unchanged. At t = T, the input abruptly rises to 20V. D is ON, as the voltage across C is 8V, $V_0 = 6V$ and in the interval T to $\frac{3T}{2}$ decays.

$$V_0\left(\frac{3T}{2}\right) = 6e^{-1/2} = 3.6V$$

$\therefore$ Voltage across C = 20 – (3.6+3.6) = 12.8V

and $t = \frac{3T}{2}$, $V_0 = -12.8V$

As the voltage is not going to change much during the interval $\frac{3T}{2}$ to 2T, at t = 2T, the output again returns to 3.6V

At $t = \frac{5T}{2}$

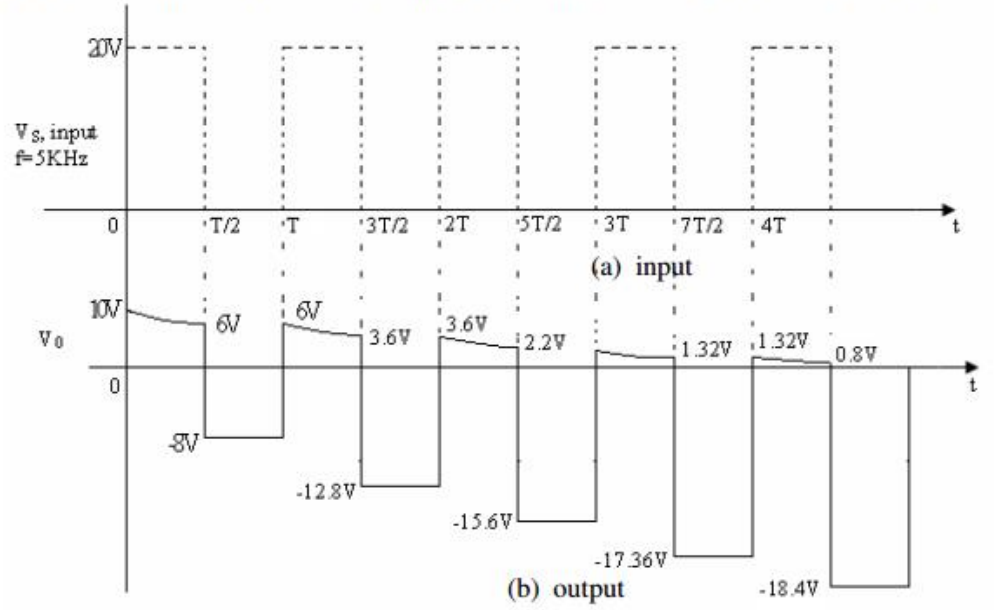
$V_0 = 3.6e^{\frac{-1}{2}} = 2.2V$

$\therefore V_A = 20 - (2.2+2.2) = 15.6V$

The output remains at -15.6V during the interval $\frac{5T}{2}$ to 3T. This again returns to 2.2V at t = 3T and decays during the interval 3T to $\frac{7T}{2}$

$V_0(\frac{7T}{2}) = 2.2e^{\frac{-1}{2}} = 1.32V$

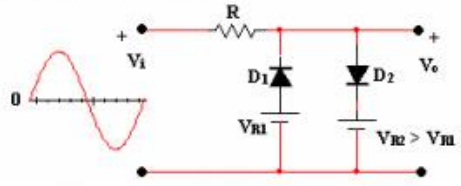
This procedure is repeated. It is seen that the output reaches the steady-state in a few cycles. i.e. the positive peaks of the input are clamped to nearly zero level at the output.



Double Diode Clipping

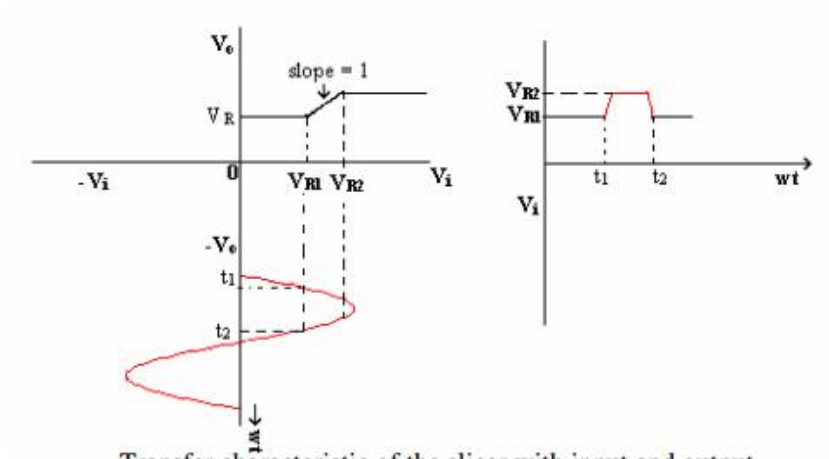
In single diode clipping circuit, the wave form is selected either above or below(but not on both sides) reference level. Two diode clippers may be used in parallel, series, or series-parallel to limit the output at two independent levels.

Consider the circuit in Fig. side



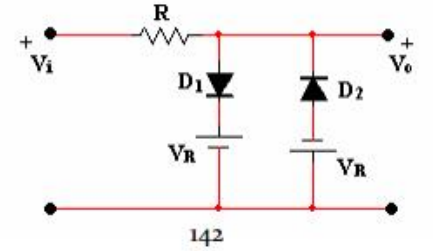
The transfer curve has two break points, one at $V_o = V_i = V_{R1}$ and a second at $V_o = V_i = V_{R2}$ has the following characteristics V_o

Input voltage	Output voltage	Diode states
$V_i \geq V_{R2}$,	$V_o = V_{R1}$	D_1 is OFF and D_2 is ON,
$V_i \leq V_{R1}$,	$V_o = V_i$	D_1 is ON D_2 is OFF,
$V_{R1} < V_i < V_{R2}$,	$V_o = V_{R2}$	D_1 and D_2 are OFF

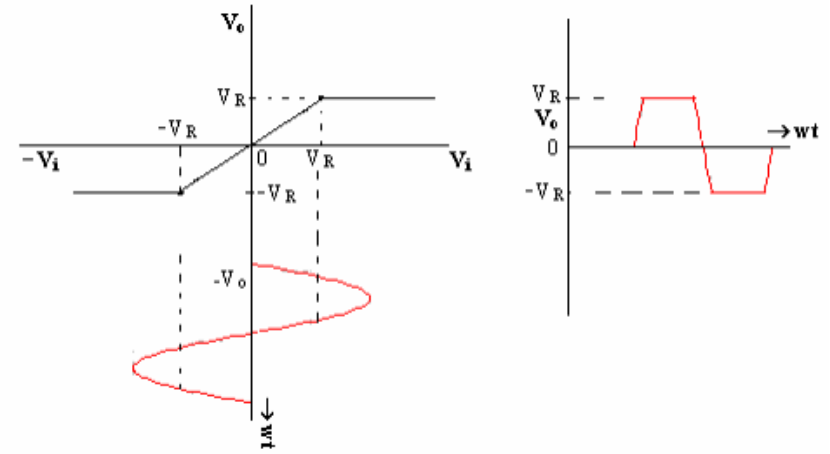


Transfer characteristic of the slicer with input and output

A combination of a positive peak clipper and a negative peak clipper, clipping the input symmetrically at the top and the bottom is called a limiter.

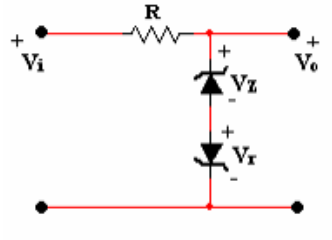


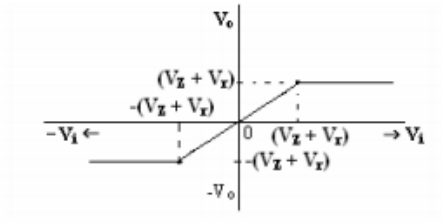
The resultant transfer characteristic is as shown below.



Transfer characteristic of a Limiter with input and output

Two avalanche diodes in series opposing, as indicated in fig below constitutes another form of double-ended clipper. If the diodes have identical characterictics then a symmetrical limiter is obtained. If the breakdown (zener) voltage is V_Z and if the cutin voltage in the forward direction is V_y, then the transfer characteristic is as shown below.

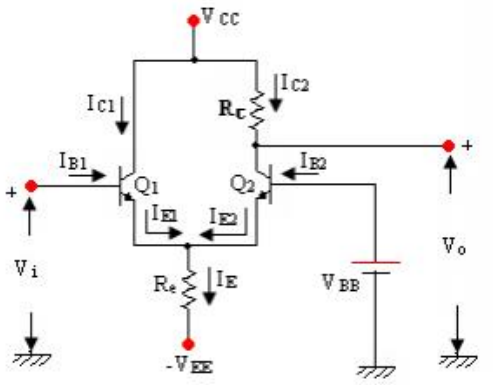




Transfer characteristic

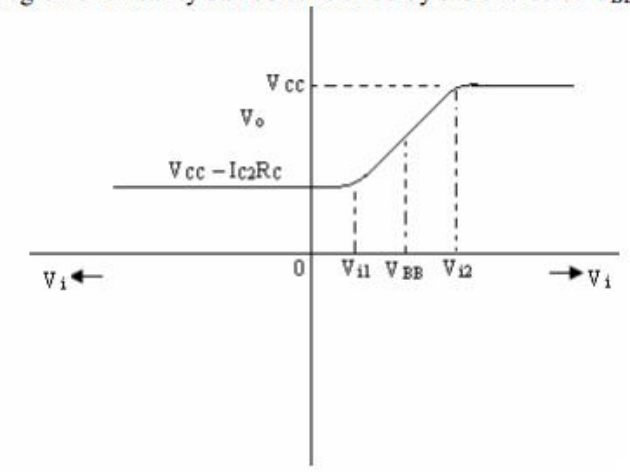
Emitter-coupled transistor clipper:

Consider initially that the input voltage V_i is negative enough to ensure that Q_1 is in cutoff .Then only Q_2 is carrying current. Consider that V_{BB} has been adjusted so that $Q_2$is in its active region. As V_i increases Q_1 will eventually come out off cutoff, both transistors will be carrying current and the input signal will appear at the output, amplified but not inverted. As V_i continues its excursion in the positive direction the common emitter will follow the base of Q_1.The base of Q_2 is fixed, a point will be reached when the rising emitter cuts off Q_2 .Finally , the input signal is amplified but twice limited, once by the cutoff of Q_1 and once by the onset of cutoff in Q_2.



A two-level transistor clipper

The transfer characteristic is shown in fig below. Thus this circuit behaves as a two-level clipper. The region of linearity can be controlled by the choice of V_{BB}.



COMPARATORS:

A comparator circuit is one which may be used to mark the instant when an arbitrary waveform attains some reference level. Consider the simple clipping circuit for comparison operation.

For the sake of explanation let the input signal be a ramp as shown below.

This input crosses the voltage level $v_i = V_R$ at time $t = t_1$.

The output remains quiescent at $v_o = V_R$ until $t = t_1$ after which it rises with the input signal

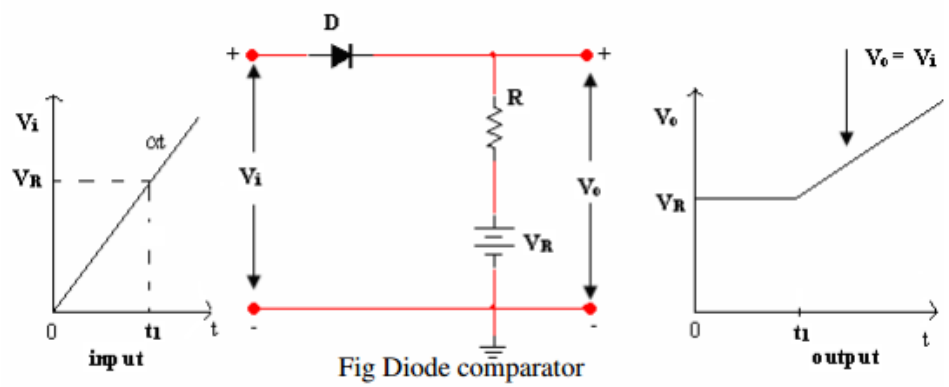
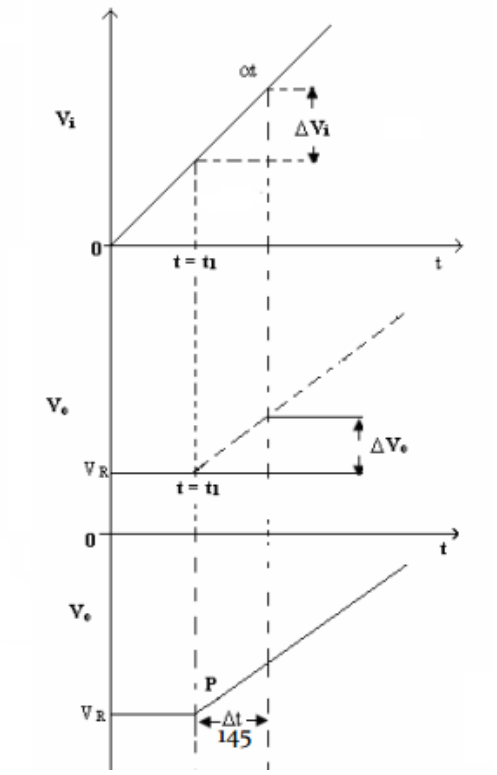


Fig Diode comparator

There is a sudden change in the slope of the output at the instant the input reaches V_R. But due to ageing and due to temperature variations the diode, may not switch from OFF to ON at exactly $t = t_1$ .It may switch state at any instant after t_1 and before t_2.



Input and output of the diode comparator

Hence, the break point (point at which device D changes state) may not exactly be at t_1 but instead, there is a break region (t_1 to t_2) .. Hence, there is a region of uncertainty which also, after the break point, the output follows the input i.e. has the same slope of the input. If this region of uncertainty is to be reduced, the response after the break point should be sharp. To achieve this amplifier may be placed before or after the comparator.

Consider the comparator circuit the response .To the left of the break point, the diode is OFF then the reverse incremental resistance of the diode, R_r is very much larger when compared to R. To the right of the break point the forward incremental resistance of the diode, R_f is very much smaller than R. If the break point is located at a point where $r = R$.

$$\Delta V_o = \Delta V_i \frac{R}{r+R} \approx V_i \quad \text{if } R >> r$$

As $\Delta V_o = \Delta V_i \dfrac{R}{r+R}$

if $r = R$

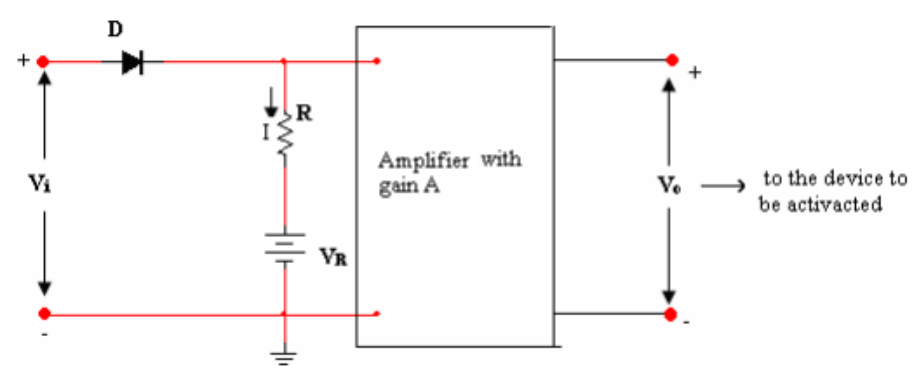
$$\therefore \frac{\Delta V_o}{\Delta V_i} = \frac{R}{R+R} = \frac{1}{2}$$

So the improvement is only half.

If a device is connected at the output of the comparator, this is required to be activated when the diode current is say, I and has a drop across R as IR.

If now an amplifier is connected at the output of the comparator so that this amplifier output activates the device.

Let the amplifier have a gain A. During $\Delta t = t_2 - t_1$, the output changes by $\Delta V_o = V_2 - V_R$, the delay in response is reduced to $\dfrac{\Delta t}{A}$ *or* $\dfrac{(t_2 - t_1)}{A}$



Output of the comparator connected to an amplifier

Let the amplifier only amplify the change in the comparator input but not the reference voltage. The device to be activated is activated only when the drop across R is IR.But now I = I/A, Hence the device is activated when the drop across R is RI/A since the diode

current is amplified by A and the diode resistance is r = $\eta V_T/I$ i.e the dynamic resistance which varies inversely with current. Therefore it is evident that, the device to be activated by the comparator will respond at a current such that r = RA

$$\therefore \quad \frac{\Delta V_o}{\Delta V_i} = A \frac{R}{r+R} = \frac{AR}{R+RA} = \frac{A}{1+A}$$

As $A \to \infty$, $\frac{\Delta V_o}{\Delta V_i} \to 1$

Without an amplifier $\frac{\Delta V_o}{\Delta V_i}$ (the transmission gain) was ½ and with an amplifier connected , $\frac{\Delta V_o}{\Delta V_i}$ is 1.Which says that there is no marked improvement in the response of the comparator arrangement .

Some applications of comparators:

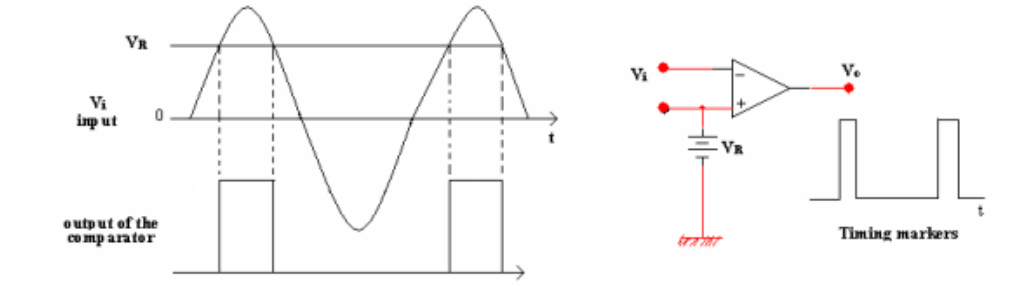
(i) **Measurement of time delays:**

In the comparator shown before, if V_{R1} is the reference level in the first comparator (double differentiator) then a pulse is generated with a peak at $t = t_1$. If V_{R2} is the reference level set in a second comparator then the pulse is generated with peak at $t = t_2$.

Then the time difference between the two pulses is simply

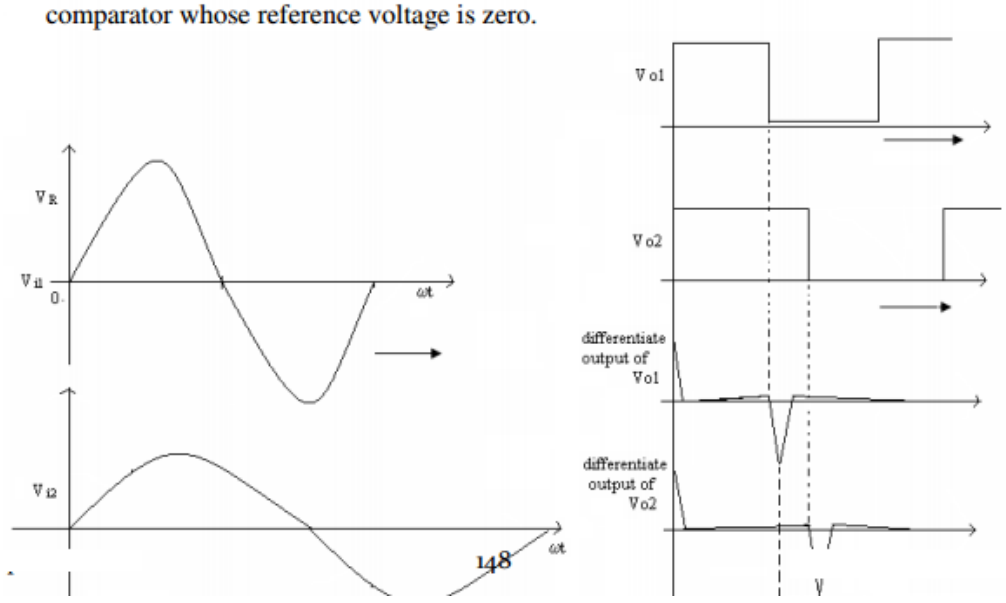
$$t_2 - t_1 = (V_{R2} - V_{R1})/\alpha$$

(ii) **Timing markers generated from sine wave:**



If a sine wave is applied as input, when the input reaches V_R output of the comparator is high till again the input reaches V_R. Differentiate and clip negative spikes. We have positive spikes which can be implemented as timing markers.

(iii) **Phase meter:** Let two sinusoidal inputs having a phase difference be applied to a comparator whose reference voltage is zero.



The output pulses are differentiated and the time difference between the outputs spikes is proportional to the phase difference.

(iv) **Square waves from sine waves**: In regenerative comparator (Schmitt trigger) if the reference voltage is $\pm$ V_{ref}, the output goes to +V or -V.